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Diodes Incorporated for Discrete and Analog Semiconductors

QPAK/PPAP – 2113

Qualification Report

Manufacturer No.:	**PCN-2113 – Conversion to Copper Bond Wire and Qualification of Additional Wafer Source on Selected Discrete Products**
Revision	**0**
Date:	**November 7, 2013**
Qualified By:	**Diodes Incorporated**
Also Applicable To:	**The part numbers listed in the associated PCN are Qualified by Similarity (QBS) to the devices included in this report.**

Please go to www.diodes.com for current data sheets on the parts listed in this report.

Prepared By:	**Diodes US Document Control**	**Date**	**November 7, 2013**
Approved By:	**Diodes US QRA Department**	**Date**	**November 7, 2013**

DIODES INCORPORATED
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www.diodes.com

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DATE: 7th November, 2013

PCN #: 2113

PCN Title: Conversion to Copper Bond Wire and Qualification of Additional Wafer Source on Selected Discrete Products

Dear Customer:

This is an announcement of change(s) to products that are currently being offered by Diodes Incorporated.

We request that you acknowledge receipt of this notification within 30 days of the date of this PCN. If you require samples for evaluation purposes, please make a request within 30 days as well. Otherwise, samples may not be built prior to this change. Please refer to the implementation date of this change as it is stated in the attached PCN form. Please contact your local Diodes sales representative to acknowledge receipt of this PCN and for any sample requests.

The changes announced in this PCN will not be implemented earlier than 90 days from the notification date stated in the attached PCN form.

Previously agreed upon customer specific change process requirements or device specific requirements will be addressed separately.

For questions or clarification regarding this PCN, please contact your local Diodes sales representative.

Sincerely,

Diodes Incorporated PCN Team

PRODUCT CHANGE NOTICE PCN-2113 REV00

Notification Date:	Implementation Date:	Product Family:	Change Type:	PCN #:
7th November, 2013	6th February, 2014	Discrete Semiconductors	Bond Wire Material / Wafer FAB Material	**2113**

TITLE

Conversion to Copper Bond Wire and Qualification of Additional Wafer Source on Selected Discrete Products

DESCRIPTION OF CHANGE

This PCN is being issued to notify customers that Diodes has qualified Copper bond wire for the part numbers listed in this PCN. In order to accommodate the Copper bond wire, the top metal composition and/or top metal thickness of the wafer has also been modified. Diodes Incorporated has also qualified an additional wafer source, Diodes internal FabTech Inc. (KFAB), for the products listed in Table 1.

Full electrical characterization and high reliability testing has been completed on representative part numbers built using Copper bond wire and/or alternative wafer source to ensure there is no change to device functionality or electrical specifications in the datasheet.

There will be no change to the Form, Fit, or Function of affected products.

IMPACT

There is no change in datasheet parameters and product performance.

PRODUCTS AFFECTED

Please refer to Table 1 for Cu bond wire conversion and additional wafer source

Please refer to Table 2 for Cu bond wire conversion

WEB LINKS

Manufacturer's Notice:	http://www.diodes.com/quality/pcns
For More Information Contact:	http://www.diodes.com/contacts
Data Sheet:	http://www.diodes.com/products

DISCLAIMER

Unless a Diodes Incorporated Sales representative is contacted in writing within 30 days of the posting of this notice, all changes described in this announcement are considered approved.

Table 1 - Cu Bond Wire Conversion and Additional Wafer Source				
DSS20201L-7	ZXTN19060CGTA	ZXTN25020DZTA	ZXTP19100CGTA	ZXTP25100CFHTA
DSS4240T-7	ZXTN19100CGTA	ZXTN25040DFHTA	ZXTP19100CZTA	ZXTP25012EFHTA
DSS4320T-7	ZXTN19100CZTA	ZXTN25040DZTA	ZXTP2006E6TA	ZXTP25140BFHTA
ZX5T2E6TA	ZXTN2005ZTA	ZXTN25050DFHTA	ZXTP2008ZTA	ZXTP25015DFHTA
ZX5T955ZTA	ZXTN2007ZTA	ZXTN25060BFHTA	ZXTP2012ZTA	ZXTP25020BFHTA
ZXGD3001E6TA	ZXTN2010ZTA	ZXTN25060BZTA	ZXTP2013ZTA	DSS20200L-7
ZXGD3002E6TA	ZXTN2011ZTA	ZXTN25100BFHTA	ZXTP2014GTC	ZXTP25020CFHTA
ZXGD3004E6TA	ZXTN25012EFHTA	ZXTN25100DFHTA	ZXTP2014ZTA	ZXTP25020DFLTA
ZXT13P20DE6TA	ZXTN25012EZTA	ZXTN25100DGTA	ZXTP25012EZTA	ZXTP25020DFHTA
ZXTC2061E6TA	ZXTN25015DFHTA	ZXTN25100DZTA	ZXTP25020DGTA	ZXTP25040DFLTA
ZXTC2062E6TA	ZXTN25020BFHTA	ZXTP19020DGTA	ZXTP25020DZTA	DSS5240T-7
ZXTC2063E6TA	ZXTN25020CFHTA	ZXTP19020DZTA	ZXTP25040DZTA	ZXTP25040DFHTA
ZXTN19020DGTA	ZXTN25020DFHTA	ZXTP19060CGTA	ZXTP25100CZTA	ZXTP25060BFHTA
ZXTN19055DZTA	ZXTN25020DGTA	ZXTP19060CZTA	ZXTP25100BFHTA	

Table 2 - Cu Bond Wire Conversion				
2DA1201Y-7	DCP69A-13	DCX124EK-7	ZXT10P12DE6TA	BC817-40W-7
2DD2679-13	DCX69-13	DCX124EK-7-F	ZXT10P20DE6TA	BC847CW-13-F
DSS30101L-7	DPLS350E-13	DCX144EK-7	ZXT10P40DE6TA	DN350T05-7
DSS4160T-7	DPLS350Y-13	DDC123JK-7-F	ZXT13N15DE6TA	DNLS160-7
ZXTN649FTA	DPLS4140E-13	DIMD10A-7	ZXT13N20DE6TA	MMBT123S-7-F
ZXTP4003ZTA	DXT5401-13	DMMT2907A-7	ZXT13N50DE6TA	MMBT5551-7-F
2DA1213O-13	DXT751-13	DMMT5401-7-F	ZXT13P12DE6TA	MMBTA13-7-F
2DA1213Y-13	DXTA92-13	DMMT5551-7-F	ZXT13P40DE6TA	MMBTA14-7-F
2DB1119S-13	DZT2907A-13	DMMT5551S-7-F	ZXTD09N50DE6TA	MMBTA28-13-F
2DB1132P-13	DZT5401-13	DRDC3105E6-7	ZXTD2090E6TA	MMBTA28-7-F
2DB1132R-13	DZT591C-13	IMT17-7	ZXTD4591E6TA	MMBTA42-7-F
2DB1188P-13	DZT751-13	IMX8-7-F	ZXTD6717E6TA	MMST5551-7-F
2DB1188R-13	DZT951-13	MMDTA06-7	2DC2412R-7	MMSTA05-7-F
2DB1386R-13	DZT953-13	MMDTA42-7-F	BC817-16-7-F	MMSTA13-7-F
2DB1424R-13	DZT955-13	ZXGD3003E6TA	BC817-16W-7	MMSTA42-7-F
DCP69-13	DZTA92-13	ZXT10N15DE6TA	BC817-25-7-F	BC807-16-7-F
DCP69-16-13	DCX114YK-7	ZXT10N20DE6TA	BC817-25W-7	BC807-16W-7
DCP69-25-13	DCX114YK-7-F	ZXT10N50DE6TA	BC817-40-7-F	BC807-25-7-F

Table 2 - Cu Bond Wire Conversion				
BC807-25W-7	DZT853-13	DDTA113TCA-7-F	MMBD914-13-F	ZXMP4A57E6TA
BC807-40-7-F	DZTA42-13	DDTA113ZCA-7-F	MMBD4148-13-F	ZXMP6A17E6TA
BC807-40W-7	DZT3150-13	DDTA114ECA-7-F	BZT52C10LP-7B	ZVN4525E6TA
DP350T05-7	DZT658-13	DDTA114WCA-7-F	BZT52C15LP-7	ZVP4525E6TA
DPLS160-7	BCV46TA	DDTA114YCA-7-F	BZT52C18LP-7	ZXMN2AMCTA
DPLS320A-7	BCW68HTA	DDTA115ECA-7-F	BZT52C22LP-7	ZXMC3AMCTA
MMBT4403-13-F	FMMT549ATA	DDTA123ECA-7-F	BZT52C2V4LP-7B	ZXMN3AMCTA
MMBT4403-7-F	FMMT549TA	DDTA123JCA-7-F	BZT52C2V7LP-7B	ZXMC4A16DN8TA
MMBT5401-7-F	FMMT589TA	DDTA124ECA-7-F	BZT52C3V9-13-F	FSV064TC
MMBTA55-7-F	FMMT591ATA	DDTA124TCA-7-F	BZT52C3V9LP-7	ZXMN10A09KTC
MMBTA56-7-F	FMMT591ATC	DDTA143ECA-7-F	BZT52C4V3LP-7	ZXMN10A25KTC
MMBTA63-7-F	FMMT591TA	DDTA143FCA-7-F	BZT52C4V7LP-7B	ZXMN15A27KTC
MMBTA64-7-F	FMMT593TA	DDTA143TCA-7-F	BZT52C7V5LP-7	ZXMN20B28KTC
MMBTA92-7-F	FMMT593TC	DDTA143XCA-7-F	BZT52C9V1LP-7	ZXMN3A04KTC
MMST4403-7-F	FMMT717TA	DDTA143ZCA-7-F	GDZ5V6LP3-7	ZXMN4A06KTC
MMST5401-7-F	FMMT718TA	DDTA144ECA-7-F	GDZ6V0LP3-7	ZXMN6A08KTC
MMSTA06-7-F	FMMT718TC	DDTA144TCA-7-F	GDZ6V2LP3-7	ZXMN6A09KTC
MMSTA55-7-F	FMMT720TA	DDTA144VCA-7-F	GDZ6V8LP3-7	ZXMN6A25KTC
MMSTA56-7-F	FMMT722TA	DDTA144WCA-7-F	GDZ7V5LP3-7	ZXMP10A16KTC
MMSTA92-7-F	FMMT723TA	DDTB113EC-7-F	GDZ8V2BLP3-7	ZXMP10A18KTC
2DD1621T-13	FMMTA56TA	DDTB113ZC-7-F	GDZ8V2LP3-7	ZXMP4A16KTC
2DD1664R-13	FMMTA92TA	DDTB114EC-7-F	ZXMN10A07ZTA	ZXMP6A16KTC
2DD1766P-13	FMMTL717TA	DDTB122LC-7-F	ZXMN6A07ZTA	ZXMP6A17KTC
2DD1766R-13	FMMTL718TA	DDTB122TC-7-F	ZXMN6A11ZTA	ZXMP6A18KTC
2DD2098R-13	ZXTP2039FTA	DDTB123EC-7-F	ZXMN3A01ZTA	ZXMP7A17KTC
DCP68-13	ZXTP2039FTC	DDTB123YC-7-F	ZXMN10A08E6TA	BAS40LP-7
DCX68-13	ZXTP2041FTA	DDTB133HC-7-F	ZXMN10A08E6TC	BAS70LP-7B
DCX68-25-13	ZXTP5401FLTA	DDTB142JC-7-F	ZXMN10B08E6TA	BAT54LP-7
DNLS320E-13	FMMT551TA	DDTB142TC-7-F	ZXMN2A01E6TA	BAT54LP-7
DNLS350E-13	FMMT555TA	BAV70-7-F	ZXMN2A03E6TA	SDM20U30LP-7
DNLS350Y-13	FMMT555TC	BAV70-13-F	ZXMN2B03E6TA	1N6263W-7-F
DXT5551-13	FMMT734TA	BAV70W-7-F	ZXMN2088DE6TA	BAT46W-7-F
DXTA42-13	FMMT596TA	BAV70T-7-F	ZXMN3A01E6TA	SD101AW-7-F
DZT491-13	ZXTP749FTA	BAV70-7-F	ZXMN3A03E6TA	SD101BW-7-F
DZT851-13	DSS5160T-7	BAV70W-7-F	ZXMN6A08E6TA	SD101CW-7-F

Table 2 - Cu Bond Wire Conversion				
SD103AW-13-F	BAS40W-04-7-F	ZLLS2000TA	MMBD2004S-7-F	BAV20WS-7-F
SD103AW-7-F	BAS40W-05-7-F	SDM20N40A-7	MMBD3004S-7-F	BAV21WS-7-F
SD103BW-13-F	BAS40W-06-7-F	SDM40E20LA-7	MMBD3004A-7-F	BAV3004WS-7
SD103BW-7-F	BAS40W-7-F	SDM40E20LS-7-F	MMBD3004C-7-F	BAS21T-7-F
SD103CW-13-F	BAS70W-04-7-F	SDM40E20LC-7	BAS19W-7-F	BAV19WS-13-F
SD103CW-7-F	BAS70W-05-7-F	ZLLS1000TA	BAS20W-7-F	BAS521-7
1N5711WS-7-F	BAS70W-06-7-F	ZLLS500TA	BAS21W-7-F	BAS521LP-7
ZLLS400TC	BAS70W-7-F	ZLLS500TC	MMBD2004SW-7-F	BAW101S-7
SD101AWS-7-F	BAT54W-13-F	SDM02U30LP3-7B	BAS20DW-7	BAW101V-7
SD101BWS-7-F	B140WS-7	BAS19-7-F	BAS21DW-7	MMBD3004S-13-F
SD101CWS-7-F	SD103AWS-7-F	BAS20-7-F	BAV19W-7-F	UDZ5V6B-7
BAT54ATA	SD103BWS-7-F	BAS21-7-F	BAV20W-7-F	UDZ5V6B-13
BAT54CTA	SD103CWS-7-F	BAV23A-7-F	BAV21W-7-F	
BAT54STA	ZLLS410TA	BAV23C-7-F	BAV3004W-7-F	
BAT54TA	SD103ASDM-7-F	BAV23S-7-F	BAV19WS-7-F	

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	2DB1184Q-13	**Lead material type**	12SnOFC-H
Package Type	TO252-3L	**Lead Material manufacturer**	Hitachi
DIE P/N	A5907F	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	TO252-3L (Spot Ag)
Wafer Diameter	5 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Phenitec	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSi
Die attach Method / Material	EPOXY/8200TI	**Front metal thickness (Top layer)**	3.5um
Bond wire material & dia.	Copper Wire,1.5mil	**Back metal type (All layers)**	Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	1.2um
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	1.01*1.01*0.23mm
Package material type	EME-G700	**Die passivation thickness range**	9000A
Package material manufacturer	SUMITOMO	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	November 7, 2012	Bill Tian	November 7, 2012
Signature				
Title				

Reliability Test Summary

FACTORY: SKE / DSH	PART NUMBER:	CUSTOMER:
	Package: TO252	DIODES INC.:2DB1184Q SWB0809023
LABORATORY (If Different): SKE	PART DESCRIPTION: Phenitec wafer:A5907F,2.0mil Copper Wire,PPAP	

DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec			NA	
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	385	0/385	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C NPN 3904 Section Characteristic BVCBO@IC=-50uA, IE=0 Characteristic BVCEO@IC=-1mA, IB=0 Characteristic BVEBO@IE=-50uA, IC=0 Characteristic ICBO@VCB=-40V, IE=0	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	NA	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vc=48V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vc=48V, PER JESD22 A-108	1	77	0/77	
	Final	T=150*C Vc=48V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=48V	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=85*C RH=85% Vc=48V	1	77	0/77	
	Final 1000 Hours	T=85*C RH=85% Vc=48V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=40V Ic=28mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8kV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30	NA	
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30	NA	
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C@30sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	10	0/10	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	10	0/10	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	5	0/5	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 11/17/08	Approved by: Susan Ding 11/17/08				

CERTIFICATION OF DESIGN AND CONSTRUCTION (for analog product)

Assembly and Test Site	Shanghai Kaihong Electronic Co., Ltd. DIODES INC. IN SHANGHAI	**Glass transition temperature (T_G)**	NA
User P/N	A0221H0 for AH1806, A0221G0 for AH1808	**Lead material type**	SOT-666G
Generic P/N	MICROPOWER OMNIPOLAR HALL-EFFECT SENSOR SWITCH	**Lead Material manufacturer**	NBKQ
Supplier P/N	AH1806-Z/AH1808-Z_SOT553	**Lead plating/ coating**	Green
Die line or process	CMOS 5V, 0.5um, 2P2M	**Lead frame material type**	ETCHING
Wafer Diameter	6 inch	**Header plating (Die land area)**	NA
Wafer Fab Site(s)	NTC	**Max junction temperature(T_j)**	NA
ID method (multiple sites)		**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road,Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	NA
Test Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road,Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAIPlant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type**	AlCu
Die attach Method / Material	WBC/8006NS	**Front metal thickness**	20kA
Bond wire material & dia.	Cu 0.8mil	**Back metal type (All layers)**	NA
Bond type (at die)	NA	**Back metal thickness (all Layers)**	NA
Bond type (at lead frame)	NA	**Die conforming coating**	No
No. of bonds over active area	3	**Die size (width x length x thickness) in um**	1050*700***140**
Mold compound material type	CEL-1702HF9SK	**Die passivation thickness range**	Oxide 4kA, SiN 6kA
Mold compound material manufacturer	HITACHI	**No. of mask steps**	**16** Layers

Diodes Inc.–HsinChu (DHC)
2F, No.24-2 Gpngyedong 4th Rd.,
Hsinchu Science Park, Hsinchu, Taiwan
886-3-5678234 www.diodes.com
Effective Date: 05/16/08
Print Date: 11/6/13 11:15 AM
RD10-3-001-01-B

CERTIFICATION OF DESIGN AND CONSTRUCTION (for analog product)

Assembly and Test Site	Shanghai Kaihong Electronic Co., Ltd. DIODES INC. IN SHANGHAI	**Glass transition temperature (T_G)**	NA
User P/N	A0221J0 for AH1807, A0221I0 for AH1809	**Lead material type**	SOT-666G
Generic P/N	MICROPOWER OMNIPOLAR HALL-EFFECT SENSOR SWITCH	**Lead Material manufacturer**	NBKQ
Supplier P/N	AH1807-Z/AH1809-Z_SOT553	**Lead plating/ coating**	Green
Die line or process	CMOS 5V, 0.5um, 2P2M	**Lead frame material type**	ETCHING
Wafer Diameter	6 inch	**Header plating (Die land area)**	NA
Wafer Fab Site(s)	NTC	**Max junction temperature(T_j)**	NA
ID method (multiple sites)		**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road,Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	NA
Test Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road,Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAIPlant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type**	AlCu
Die attach Method / Material	WBC/8006NS	**Front metal thickness**	20kA
Bond wire material & dia.	Cu 0.8mil	**Back metal type (All layers)**	NA
Bond type (at die)	NA	**Back metal thickness (all Layers)**	NA
Bond type (at lead frame)	NA	**Die conforming coating**	No
No. of bonds over active area	3	**Die size (width x length x thickness) in um**	1050*700***140**
Mold compound material type	CEL-1702HF9SK	**Die passivation thickness range**	Oxide 4kA, SiN 6kA
Mold compound material manufacturer	HITACHI	**No. of mask steps**	**16** Layers

Diodes Inc.–HsinChu (DHC)
2F, No.24-2 Gpngyedong 4th Rd.,
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RD10-3-001-01-B

Test Summary

QP # 13012401

Description: AH1806-Z-7/AH1808-Z-7/AH1807-Z-7/AH1809-Z-7(SOT553_Cu wire conversion)

			Eval Device 1		QBS Device 1		QBS Device 2	
	Part Number		AH1806-Z/AH1808-Z AH1807-Z/AH1809-Z		AH1806-Z/AH1808-Z		AH1807-Z/AH1809-Z	
	Package		SOT553		SOT553		SOT553	
	Package Size		1.6*1.6*0.58mm		1.6*1.6*0.58mm		1.6*1.6*0.58mm	
	Die Name(s)		A0221H0 / A0221G0 A0221J0 / A0221I0		A0221F0(MOW wafer)		A0221J0 / A0221I0	
	Wafer FAB		NTC		NTC		NTC	
	Wafer Diameter		6"		6"		6"	
	Bond Type (at Die)		NA		NA		NA	
	Bond Type (at LF)		NA		NA		NA	
	No. of bond over active area		3		3		3	
	Glass Transistion Temp		NA		NA		NA	
	Lead Material Manufacture		NBKQ		NBKQ		NBKQ	
	Header plating (Die Land Area)		NA		NA		NA	
	Max Junction Temp		NA		NA		NA	
	Max Thermal resistance Junc (case)		NA		NA		NA	
	Max Thermal resistance Junc (amibent)		NA		NA		NA	
	Front Metal Type		AlCu		AlCu		AlCu	
	Back Metal Type (All Layers)		N/A		N/A		N/A	
	Back Metal Thickness (All Layers)		N/A		N/A		N/A	
	Die Conforming Coating		No		No		No	
	Die passivation thickness range		Oxide 4kA, SiN 6kA		Oxide 4kA, SiN 6kA		Oxide 4kA, SiN 6kA	
	No of masks Steps		16		16		16	
	Wafer Lot#		NA		NA		NA	
	SWR#		NA		NA		NA	
	Assembly Lot #		NA		NA		NA	
	Die Size (W/L/Thickness)		1.05*0.7mm		1.05*0.7mm		1.05*0.7mm	
	Die Process / Technology		CMOS 5V, 0.5um, 2P2M		CMOS 5V, 0.5um, 2P2M		CMOS 5V, 0.5um, 2P2M	
	Die Quantity (eg. Die per package)		1		1		1	
	DB Epoxy/Solder Type		WBC		WBC		WBC	
	Die Attach Material		8006NS		8006NS		8006NS	
	Wire Bond Material (Au, Cu, Al)		Cu		Au		Au	
	Wire Diameter		0.8mil		1mil		1mil	
	Front Metal Thickness		2um		2um		2um	
	Leadframe Type		SOT-666G		SOT-666G		SOT-666G	
	Leadframe Material		ETCHING		ETCHING		ETCHING	
	Molding Compound Type		CEL-1702HF9SK		CEL-1702HF9SK		CEL-1702HF9SK	
	Green Compound (Yes/No)		Yes		Yes		Yes	
	Lead-Free (Yes/No)		Yes		Yes		Yes	
	Assembly Site		SAT		SAT		SAT	
	Test Site		SAT		SAT		SAT	
	DataSheet		AH1806 / AH1808 AH1807 / AH1809		AH1806 / AH1808		AH1807 / AH1809	

Realibility Testing

Test	Test Conditions	Duration / Limits	Fail/SS	X = Test Needed	Results Pass/Fail	QBS Test Completed	Results Pass/Fail	QBS Test Completed	Results Pass/Fail
MSL1 Pre-cond	Bake 125C	24 Hrs	0/154	X	Pass	X	Pass		
	Soak 85C, 85% RH	168Hrs	0/154	X	Pass	X	Pass		
	IR reflow 260C	3 cycles	0/154	X	Pass	X	Pass		
HTOL	Tj>125C, 100% Vcc	168 Hrs	0/77			X	Pass	X	Pass
		500 Hrs	0/77			X	Pass	X	Pass
		1000 Hrs	0/77			X	Pass	X	Pass
TC	-65C-150C	500 cycles	0/77	X	Pass	X	Pass		
		1000 cycles	0/77	X	Pass				
HAST	130C, 85%RH 33.3 psia 80% Bias	96 Hrs	0/77	X	Pass	X	Pass		
AC	T=121°C 15PSIG 100%RH	96 Hrs	0/77						
HTSL	150C	168 Hrs	0/77	X	Pass	X	Pass		
		500 Hrs	0/77	X	Pass	X	Pass		
		1000 Hrs	0/77	X	Pass	X	Pass		
Latch-up	JESD78	100mA	0/6			X	Pass	X	Pass
ESD	HBM (AEC-Q100-002)	+-2KV	0/3			X	Pass	X	Pass
	MM (AEC-Q100-003)	+-200V	0/3			X	Pass	X	Pass
WBP	MIL-STD883-2011	Cpk>1.66	0/30	X	Pass	X			
WBS	JESD22-B116B	Cpk>1.66	0/30	X	Pass	X			

CERTIFICATE OF DESIGN AND CONSTRUCTION

Printed specifications are not controlled documents. Verify revision before using.

Assembly and Test Site	DIODES INC	**Glass Transition Temperature (T_G)**	120℃
DIC P/N	AZ23C20-7-G-89	**Lead Frame Type**	SOT-23A
Package Type	SOT-23	**Lead Frame Manufacturer**	MHT/PBE/VAST/XMYH/NBKQ
DIE P/N	Z5200	**Lead Frame Material**	Alloy42
Die Line or Process	ZENER	**Terminal Finish (Plating) Material**	100% tin, Pb free
Wafer Diameter	5"	**Header Plating (Die Land Area)**	Spot Ag
Wafer Fab Site(s)	KFAB	**Max Junction Temperature (T_j)**	150℃
ID Method (multiple sites)	N/A	**Max Thermal Resistance Junction to Case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max Thermal Resistance Junction to Ambient (θ_{JA})***	417°C/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front Metal Type (Top Layer)**	Al-1%Si
Die attach Method / Material	EUTECTIC	**Front Metal Thickness (Top Layer)**	20kA
Bond Wire/Clip Material & Wire Diameter	Copper wire,1.0mil	**Back Metal Type (All Layers)**	NiV-Au
Bond Type (at top side of the die)	Thermo sonic	**Back Metal Thickness (all Layers)**	NiV-125A, Au-5150A
Bond Type (at leadframe)	Thermo sonic	**Die Conformal Coating (Passivation)**	N/A
No. of Bonds over Active Area	2	**Die Passivation Thickness Range**	6000-9000A
Mold Compound Material Type	GR640HV-L1	**Die Size (Width x Length x Thickness) in mm**	0.35*0.35*0.216mm
Mold Compound Material Manufacturer	HENKEL	**No. of Mask Steps**	4

Completed by		**Date**	**Certified by**	**Date**
Typed/Printed	Jenny Liu	July 17, 2013	Bill Tian	7/17/2013
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY: SAT		PART NUMBER :AZ23C20-7-G-89 SWR1307085 Package:SOT23 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION: For NY qual,Z5200/1.0Cu/ GR640HV-1				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VZ@IZT=5mA Characteristic Zzt@Izt=5mA Characteristic Zzk@Izk=1mA Characteristic VR@IR=0.1uA	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vz=16V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vz=16V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vz=16V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	
7.3.5.7 (9)	HAST	T=130*C RH=85% Vz=16v	1	77		
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vz=16v	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=21v/Iz=15mA, PER MIL-STD-750 METHOD 1037				15000cy @2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560CY	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000CY	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	MM pass 400V HBM pass 2kV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	2	0/2	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	30	0/30	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	30	0/30	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	30	0/30	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 09/16/13	Approved by:Adam Gu 09/16/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110℃
DIC P/N	AZ23C5V6W-7-F	**Lead material type**	Alloy42
Package Type	SOT-323	**Lead Material manufacturer**	VAST/PBE
DIE P/N	Z5056	**Lead plating/ coating**	Pb free
Die line or process	ZENER	**Lead frame material type**	Alloy42
Wafer Diameter	5"	**Header plating (Die land area)**	Spot Ag
Wafer Fab Site(s)	FABTECH	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	NA
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-1%Si
Die attach Method / Material	EUTECTIC	**Front metal thickness (Top layer)**	20KA
Bond wire material & dia.	Cu wire, 0.8MIL	**Back metal type (All layers)**	NiV-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	125A-5150A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.35*0.35*0.216mm
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	6,000A-9,000A
Package material manufacturer	HITACHI	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Helen Wang	May 25, 2011	Robin Sun	May 25, 2011
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :AZ23C5V6W-7-F SWR1104227 SWR1106306 SWR1106307 CUSTOMER: Package:SOT323 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:FT wafer Z5056/50092991N qual;0.8Cu wire; CEL-1702HF9				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	312	0/312	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VZ@IZ=5mA Characteristic ZZT@IZ=5mA Characteristic ZZK@IZ=0.5mA Characteristic IR@VR=2.5	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=4.48V, PER JESD22 A-108	1	78		
	Pretest		1	78	0/78	
	@ 500 Hours	T=150*C Vr=4.48V, PER JESD22 A-108	1	78	0/78	
	Final 1000Hours	T=150*C Vr=4.48V, PER JESD22 A-108	1	78	0/78	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	78	0/78	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	78	0/78	96H
7.3.5.7 (9)	H3TRB	T=85*C RH=85% Vr=4.48v	1	78		
	Pretest		1	78	0/78	
	@ 500Hours	T=85*C RH=85% Vr=4.48v	1	78	0/78	
	Final 1000 Hours	T=85*C RH=85% Vr=4.48v	1	78	0/78	
7.3.5.7 (9a)	HIGHLY ACCELERATED STRESS TEST(HAST)	T=130*C RH=85% Vr=4.5v	1	78	0/78	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=5.8V/Iz=17mA, PER MIL-STD-750 METHOD 1037				
	Pretest	MIL-STD-750 METHOD 1037	1	78	0/78	
	Midpoint	MIL-STD-750 METHOD 1037	1	78	0/78	
	After	MIL-STD-750 METHOD 1037	1	78	0/78	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 8/29/11	Approved by:Adam Gu 8/29/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110℃
DIC P/N	AZ23C6V2-7-G-89	**Lead material type**	Alloy42
Package Type	SOT-23	**Lead Material manufacturer**	MHT/PBE/XMYH/VAST/NBKQ
DIE P/N	Z5062	**Lead plating/ coating**	Pb free
Die line or process	ZENER	**Lead frame material type**	Alloy42
Wafer Diameter	5"	**Header plating (Die land area)**	Spot Ag
Wafer Fab Site(s)	FABTECH	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	NA
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-1%Si
Die attach Method / Material	EUTECTIC	**Front metal thickness (Top layer)**	20kA
Bond wire material & dia.	Cu wire, 0.8MIL	**Back metal type (All layers)**	NiV-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	125A-5150A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.35*0.35*0.216mm
Package material type	*KTMC1050G	**Die passivation thickness range**	6,000A-9,000A
Package material manufacturer	KCC	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Helen Wang	May 25, 2011	Robin Sun	May 25, 2011
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :AZ23C6V2-7 SWR1104221 SWR1105307 SWR1105308 CUSTOMER: Package:DFN1006-2 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:FT wafer Z5062/50096360N1 qual;0.8Cu wire;KTMC1050G				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	312	0/312	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VZ@IZ=5mA Characteristic ZZT@IZ=5mA Characteristic ZZK@IZ=0.5mA Characteristic IR@VR=2.5	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C VZ=4.96V, PER JESD22 A-108	1	78		
	Pretest		1	78	0/78	
	@ 500 Hours	T=150*C VZ=4.96V, PER JESD22 A-108	1	78	0/78	
	Final 1000Hours	T=150*C VZ=4.96V, PER JESD22 A-108	1	78	0/78	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	78	0/78	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	78	0/78	96H
7.3.5.7 (9)	H3TRB	T=85*C RH=85% VZ=4.96v	1	78		
	Pretest		1	78	0/78	
	@ 500Hours	T=85*C RH=85% VZ=4.96v	1	78	0/78	
	Final 1000 Hours	T=85*C RH=85% VZ=4.96v	1	78	0/78	
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vz=4.96v	1	78	0/78	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=6.3V/Iz=46mA, PER MIL-STD-750 METHOD 1037				
	Pretest	MIL-STD-750 METHOD 1037	1	78	0/78	
	Midpoint	MIL-STD-750 METHOD 1037	1	78	0/78	
	After	MIL-STD-750 METHOD 1037	1	78	0/78	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 8/18/11	Approved by:Adam Gu 8/18/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	160C
DIC P/N	BAT54WS-7-F-76	**Lead material type**	Alloy 42
Package Type	SOD-323	**Lead Material manufacturer**	MHT/VAST/XMYH/NBKQ
DIE P/N	S9069	**Lead plating/ coating**	Pure Sn
Die line or process	Sky	**Lead frame material type**	SOD323A
Wafer Diameter	5 inch	**Header plating (Die land area)**	Spot Ag
Wafer Fab Site(s)	DFT	**Max junction temperature(T_j)**	150C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	248 ℃/W
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	578 ℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al/Si
Die attach Method / Material	EUTECTIC / N/A	**Front metal thickness (Top layer)**	2um
Bond wire material & dia.	Cu wire, 1.0mil	**Back metal type (All layers)**	AuNi
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	0.5um
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	N/A
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.31*0.31*0.21
Package material type	KTMC1050G	**Die passivation thickness range**	6000A to 9000A
Package material manufacturer	KCC	**No. of mask steps**	3

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

vcxbb

Completed by		Date	Certified by	Date
Typed/Printed	Caixia Wei	November 4, 2011	Robin Sun	November 4, 2011
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: BAT54WS SWR1111030 CUSTOMER: Package:SOD323 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Fabtech wafer S9069 qual,1.0Cu				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VBR @IR=100uA Characteristic VF @IF=1mA Characteristic VF @IF=10mA Characteristic VF @IF=100mA Characteristic IR @VR=30V Characteristic IR @VR=25V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/25	2.2A
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=24V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=24V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=24V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9)	H3TRB	T=85*C RH=85% Vr=24V			N/A	
	Pretest		1	77		
	@ 500 Hours	T=85*C RH=85% Vr=24V	1	77		
	@ 1000 Hours	T=85*C RH=85% Vr=24V	1	77		
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vr=24V	1	77	0/77	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=200mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	578 ℃/W
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (U	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 2/1/12		Approved by:Adam Gu 2/1/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	160℃
DIC P/N	BAV16W	**Lead material type**	Alloy 42
Package Type	SOD-123	**Lead Material manufacturer**	MHT/VAST/XMYH/NBKQ
DIE P/N	B1001F	**Lead plating/ coating**	Pb free
Die line or process	Planar Process technology	**Lead frame material type**	Alloy 42
Wafer Diameter	6"	**Header plating (Die land area)**	Ag
Wafer Fab Site(s)	FabTech	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. Diodes Shanghai Co.,Ltd	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	Diodes Shanghai Co.,Ltd	**Front metal type (Top layer)**	AlSiCu
Die attach Method / Material	Eutectic	**Front metal thickness (Top layer)**	3.5 um
Bond wire material & dia.	1.0mil copper wire	**Back metal type (All layers)**	NiV/Au
Bond type (at top side of the die)	Thermo-Ultrasonic	**Back metal thickness (all Layers)**	125A NiV+5150 Au
Bond type (at leadframe)	Thermo-Ultrasonic	**Die conforming coating**	Not specified
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.280 x 0.280 x0.216
Package material type	KTMC1050G	**Die passivation thickness range**	6000 - 9000 angstroms
Package material manufacturer	KCC	**No. of mask steps**	5

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Hill Chen	August 12, 2011	Phil Mao	August 12, 2011
Signature				
Title	Wafer Engineer		Wafer Section Manager	

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: BAV16W SWR1202168 CUSTOMER: Package:SOD123 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Fabtech wafer B1001F qual,1.0Cu				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VF @IF=1mA Characteristic VF @IF=10mA Characteristic VF @IF=50mA Characteristic VF @IF=150mA Characteristic VBR @IR=1uA Characteristic IR @VR=25V Characteristic IR @VR=75V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=80V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=80V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=80V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vr=42V	1	77	0/77	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=150mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	PASS	MM 400V HBM 4KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 5/18/12		Approved by:Adam Gu 5/18/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	160℃
DIC P/N	BAV99	**Lead material type**	Alloy 42
Package Type	SOT-23	**Lead Material manufacturer**	MHT/VAST/XMYH/PBE/NBKQ
DIE P/N	B1001F	**Lead plating/ coating**	Pb free
Die line or process	Planar Process technology	**Lead frame material type**	Alloy 42
Wafer Diameter	6"	**Header plating (Die land area)**	Ag
Wafer Fab Site(s)	FabTech	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. Diodes Shanghai Co.,Ltd	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	Diodes Shanghai Co.,Ltd	**Front metal type (Top layer)**	AlSiCu
Die attach Method / Material	Eutectic	**Front metal thickness (Top layer)**	3.5 um
Bond wire material & dia.	1.0mil copper wire	**Back metal type (All layers)**	NiV/Au
Bond type (at top side of the die)	Thermo-Ultrasonic	**Back metal thickness (all Layers)**	125A NiV+5150 Au
Bond type (at leadframe)	Thermo-Ultrasonic	**Die conforming coating**	Not specified
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.280 x 0.280 x0.216
Package material type	KTMC1050G	**Die passivation thickness range**	6000 - 9000 angstroms
Package material manufacturer	KCC	**No. of mask steps**	5

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Hill Chen	August 12, 2011	Phil Mao	August 12, 2011
Signature				
Title	Wafer Engineer		Wafer Section Manager	

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: BAV99 SWR1202176 CUSTOMER: Package:SOT23 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Fabtech wafer B1001F qual,1.0Cu				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VF @IF=1mA Characteristic VF @IF=10mA Characteristic VF @IF=50mA Characteristic VF @IF=150mA Characteristic VBR @IR=2.5uA Characteristic IR @VR=25V Characteristic IR @VR=75V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=60V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=60V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=60V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vr=42V	1	77	0/77	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=200mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	pass	MM 400V HBM 4KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 5/11/12		Approved by:Adam Gu 5/11/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110℃
DIC P/N	BAV99DW-7-F	**Lead material type**	Alloy 42
Package Type	SOT-363	**Lead Material manufacturer**	PBE
DIE P/N	B1001F	**Lead plating/ coating**	Pb free
Die line or process	Planar Process technology	**Lead frame material type**	Alloy 42
Wafer Diameter	6"	**Header plating (Die land area)**	Ag
Wafer Fab Site(s)	FabTech	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. Diodes Shanghai Co.,Ltd	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	Diodes Shanghai Co.,Ltd	**Front metal type (Top layer)**	AlSiCu
Die attach Method / Material	Eutectic	**Front metal thickness (Top layer)**	3.5 um
Bond wire material & dia.	1.0mil copper wire	**Back metal type (All layers)**	NiV/Au
Bond type (at top side of the die)	Thermo-Ultrasonic	**Back metal thickness (all Layers)**	125A NiV+5150 Au
Bond type (at leadframe)	Thermo-Ultrasonic	**Die conforming coating**	N/A
No. of bonds over active area	4	**Die size (width x length x thickness) in mm**	0.280 x 0.280 x 0.216
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	6000 - 9000 angstroms
Package material manufacturer	Hitachi Chemical	**No. of mask steps**	5

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Hill Chen	August 12, 2011	Phil Mao	August 12, 2011
Signature				
Title	Wafer Engineer		Wafer Section Manager	

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: BAV99DW SWR1202177 CUSTOMER: Package:SOT363 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Fabtech wafer B1001F qual,copper wire				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VF @IF=1mA Characteristic VF @IF=10mA Characteristic VF @IF=50mA Characteristic VF @IF=150mA Characteristic VBR @IR=2.5uA Characteristic IR @VR=20V Characteristic IR @VR=75V Characteristic IR @VR=100V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=60V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=60V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=60V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vr=42V	1	77	0/77	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=215mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	MM 400V HBM 3KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 7/3/12		Approved by:Adam Gu 7/3/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110℃
DIC P/N	BAW101	**Lead material type**	Alloy 42
Package Type	SOT-143	**Lead Material manufacturer**	MHT
DIE P/N	D1089B / D1089BT	**Lead plating/ coating**	Pb free
Die line or process	Planar Proces technology	**Lead frame material type**	Alloy 42
Wafer Diameter	5 inch	**Header plating (Die land area)**	Ag
Wafer Fab Site(s)	Fabtech	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. Diodes Shanghai Co.,Ltd	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	Diodes Shanghai Co.,Ltd	**Front metal type (Top layer)**	AlSi
Die attach Method / Material	Eutectic	**Front metal thickness (Top layer)**	3.5um
Bond wire material & dia.	1.0mil copper wire	**Back metal type (All layers)**	NiV/Au
Bond type (at top side of the die)	Thermo-Ultrasonic	**Back metal thickness (all Layers)**	125A NiV+5150 Au
Bond type (at leadframe)	Thermo-Ultrasonic	**Die conforming coating**	Not specified
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	D1089B: 0.400 x 0.400 x0.216 D1089BT: 0.400 x 0.400 x0.150
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	Not specified
Package material manufacturer	Hitachi Chemical	**No. of mask steps**	5

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Hill Chen	August 12, 2011	Phil Mao	August 12, 2011
Signature				
Title	Wafer Engineer		Wafer Section Manager	

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: BAW101-7 SWR1203086 CUSTOMER: Package:SOT143 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Fabtech wafer D1089BT qual,1.0Cu				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VBR @IR=100uA Characteristic VF @IF=1mA Characteristic VF @IF=10mA Characteristic VF @IF=100mA Characteristic IR @VR=30V Characteristic IR @VR=25V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=240V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=240V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=240V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9)	HAST	T=130*C RH=85% Vr=42V				
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vr=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=140mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000H full hirel test.					
Submitted by:Joan Yu 7/7/12		Approved by:Adam Gu 7/7/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110℃
DIC P/N	BAW101V	**Lead material type**	EFTEC-64
Package Type	SOT-563	**Lead Material manufacturer**	MHT/PBE/Hitachi-cable
DIE P/N	D1089BT	**Lead plating/ coating**	Pb free
Die line or process	Planar Proces technology	**Lead frame material type**	EFTEC-64
Wafer Diameter	5 inch	**Header plating (Die land area)**	Ag
Wafer Fab Site(s)	Fabtech	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. Diodes Shanghai Co.,Ltd	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	Diodes Shanghai Co.,Ltd	**Front metal type (Top layer)**	AlSi
Die attach Method / Material	Eutectic	**Front metal thickness (Top layer)**	3.5um
Bond wire material & dia.	1.0mil copper wire	**Back metal type (All layers)**	NiV/Au
Bond type (at top side of the die)	Thermo-Ultrasonic	**Back metal thickness (all Layers)**	125A NiV+5150 Au
Bond type (at leadframe)	Thermo-Ultrasonic	**Die conforming coating**	Not specified
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.400 x 0.400 x0.15
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	Not specified
Package material manufacturer	Hitachi Chemical	**No. of mask steps**	5

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Hill Chen	August 16, 2011	Phil Mao	August 16, 2011
Signature				
Title	Wafer Engineer			Wafer Section Manager

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: BAW101V-7 SWR1203077 CUSTOMER: Package:SOT666 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:KFAB wafer D1089BT qual,1.0Cu				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VBR @IR=100uA Characteristic VF @IF=1mA Characteristic VF @IF=10mA Characteristic VF @IF=100mA Characteristic IR @VR=30V Characteristic IR @VR=25V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=260V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=260V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=260V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9)	HAST	T=130*C RH=85% Vr=42V				
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vr=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=140mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000H full hirel test.					
Submitted by:Joan Yu 12/07/12		Approved by:Adam Gu 12/07/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110℃
DIC P/N	BZT52C3V6-7-F	**Lead material type**	ALLOY42
Package Type	SOD-123	**Lead Material manufacturer**	MHT/VAST/XMYH/NBKQ/APL
DIE P/N	Z5036	**Lead plating/ coating**	NA
Die line or process	ZENER	**Lead frame material type**	ALLOY42
Wafer Diameter	5"	**Header plating (Die land area)**	Spot Ag
Wafer Fab Site(s)	FABTECH	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	NA
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-1%SI
Die attach Method / Material	EUTECTIC	**Front metal thickness (Top layer)**	20KA
Bond wire material & dia.	CU wire/1.0MIL	**Back metal type (All layers)**	NiV-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	125A-5150A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.35*0.35*0.216mm
Package material type	KTMC1050G	**Die passivation thickness range**	18,000A-22,000A
Package material manufacturer	KCC	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Helen Wang	May 25, 2011	Robin Sun	May 25, 2011
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :BZT52C3V6-7-F SWR1104240 SWR1105305 SWR1105306 CUSTOMER: Package:SOD123 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:FT wafer Z5036/50090990N1 qual;1.0Cu wire; KTMC1050G				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VZ@IZ=5mA Characteristic ZZT@IZ=5mA Characteristic ZZK@IZ=0.5mA Characteristic IR@VR=2.5	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=2.9V, PER JESD22 A-108	1	78		
	Pretest		1	78	0/78	
	@ 500 Hours	T=150*C Vr=2.9V, PER JESD22 A-108	1	78	0/78	
	Final 1000Hours	T=150*C Vr=2.9V, PER JESD22 A-108	1	78	0/78	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	78	0/78	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	78	0/78	96H
7.3.5.7 (9)	H3TRB	T=85*C RH=85% Vr=2.9v	1	78		
	Pretest		1	78	0/78	
	@ 500Hours	T=85*C RH=85% Vr=2.9v	1	78	0/78	
	Final 1000 Hours	T=85*C RH=85% Vr=2.9v	1	78	0/78	
7.3.5.7 (9a)	HIGHLY ACCELERATED STRESS TEST(HAST)	T=130*C RH=85% Vr=2.9v	1	78	0/78	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=4.7V/Iz=105mA, PER MIL-STD-750 METHOD 1037				
	Pretest	MIL-STD-750 METHOD 1037	1	78	0/78	
	Midpoint	MIL-STD-750 METHOD 1037	1	78	0/78	
	After	MIL-STD-750 METHOD 1037	1	78	0/78	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 8/15/11	Approved by:Adam Gu 8/15/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110℃
DIC P/N	BZT52C4V7LP-7	**Lead material type**	C7025HH
Package Type	DFN1006-2	**Lead Material manufacturer**	MHT/ASM/AMST/PBE
DIE P/N	Z5047Q	**Lead plating/ coating**	NA
Die line or process	ZENER	**Lead frame material type**	C7025HH
Wafer Diameter	5"	**Header plating (Die land area)**	Spot Ag
Wafer Fab Site(s)	FABTECH	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	NA
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-1%SI
Die attach Method / Material	Epoxy/QMI519	**Front metal thickness (Top layer)**	20KA
Bond wire material & dia.	Cu wire, 0.8MIL	**Back metal type (All layers)**	TI-NiV-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	1,500A-3,300A-1,200A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.35*0.35*0.14mm
Package material type	EME-G770HCD	**Die passivation thickness range**	18,000A-22,000A
Package material manufacturer	SUMITOMO	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Helen Wang	May 25, 2011	Robin Sun	May 25, 2011
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :BZT52C4V7LP-7 SWR1104225 SWR1106302 SWR1106303 CUSTOMER: Package:DFN1006-2 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:FT wafer Z5047Q/50092346 qual;1.0Cu wire; EME-G770HCD				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	312	0/312	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VZ@IZ=5mA Characteristic ZZT@IZ=5mA Characteristic ZZK@IZ=0.5mA Characteristic IR@VR=2.5	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C VZ=3.7V, PER JESD22 A-108	1	78		
	Pretest		1	78	0/78	
	@ 500 Hours	T=150*C VZ=3.7V, PER JESD22 A-108	1	78	0/78	
	Final 1000Hours	T=150*C VZ=3.7V, PER JESD22 A-108	1	78	0/78	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	78	0/78	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	78	0/78	96H
7.3.5.7 (9)	H3TRB	T=85*C RH=85% VZ=3.76v	1	78		
	Pretest		1	78	0/78	
	@ 500Hours	T=85*C RH=85% VZ=3.76v	1	78	0/78	
	Final 1000 Hours	T=85*C RH=85% VZ=3.76v	1	78	0/78	
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vz=3.76v	1	78	0/78	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=5V/Iz=50mA, PER MIL-STD-750 METHOD 1037				
	Pretest	MIL-STD-750 METHOD 1037	1	78	0/78	
	Midpoint	MIL-STD-750 METHOD 1037	1	78	0/78	
	After	MIL-STD-750 METHOD 1037	1	78	0/78	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 8/21/11	Approved by:Adam Gu 8/21/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110℃
DIC P/N	BZT52C51-7-01-F	**Lead material type**	Alloy42
Package Type	SOD-123	**Lead Material manufacturer**	MHT/VAST/XMYH/NBKQ/APL
DIE P/N	Z5510	**Lead plating/ coating**	Pb free
Die line or process	ZENER	**Lead frame material type**	Alloy42
Wafer Diameter	5"	**Header plating (Die land area)**	Spot Ag
Wafer Fab Site(s)	FABTECH	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	NA
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-1%Si
Die attach Method / Material	EUTECTIC	**Front metal thickness (Top layer)**	20KA
Bond wire material & dia.	Cu wire, 0.8MIL	**Back metal type (All layers)**	NiV-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	125A-5,150A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.41*0.41*0.216
Package material type	KTMC1050G	**Die passivation thickness range**	6,000A-9,000A
Package material manufacturer	KCC	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Helen Wang	May 25, 2011	Robin Sun	May 25, 2011
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :BZT52C51-7 SWR1104238/SWR1106312/6313 CUSTOMER: Package:SOD123 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:FT wafer ZT57M51/Z5510 qual,0.8Cu				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	312	0/312	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VZ@IZ=5mA Characteristic ZZT@IZ=5mA Characteristic ZZK@IZ=1.0mA Characteristic IR@VR=38	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=40.8V, PER JESD22 A-108	1	78		
	Pretest		1	78	0/78	
	@ 500 Hours	T=150*C Vr=40.8V, PER JESD22 A-108	1	78	0/78	
	Final 1000Hours	T=150*C Vr=40.8V, PER JESD22 A-108	1	78	0/78	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	78	0/78	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	78	0/78	
7.3.5.7 (9a)	HIGHLY ACCELERATED STRESS TEST(HAST)	T=130*C RH=85% Vr=41v	1	78	0/78	96H
7.3.5.7 (9)	H3TRB	T=85*C RH=85% Vr=40.8v	1	78		
	Pretest		1	78	0/78	
	@ 500 Hours	T=85*C RH=85% Vr=40.8v	1	78	0/78	
	Final 1000Hours	T=85*C RH=85% Vr=40.8v	1	78	0/78	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=62v/Iz=8mA, PER MIL-STD-750 METHOD 1037				
	Pretest	MIL-STD-750 METHOD 1037	1	78	0/78	
	Midpoint 7560CY	MIL-STD-750 METHOD 1037	1	78	0/78	
	After 15000CY	MIL-STD-750 METHOD 1037	1	78	0/78	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 9/7/11	Approved by:Adam Gu 9/7/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	DDZ43-7	**Lead material type**	Alloy 42
Package Type	SOD-123	**Lead Material manufacturer**	PBE,VAST,NBKQ,XMYH
DIE P/N	Z4430	**Lead plating/ coating**	Pb free
Die line or process	Zener	**Lead frame material type**	Alloy 42
Wafer Diameter	5inch	**Header plating (Die land area)**	NA
Wafer Fab Site(s)	DFT	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	305 ℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-1%Si
Die attach Method / Material	EUTECTIC	**Front metal thickness (Top layer)**	2um
Bond wire material & dia.	Copper Wire, 1.0mil	**Back metal type (All layers)**	Ti-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.41*0.41*0.216mm
Package material type	KTMC1050G	**Die passivation thickness range**	NA
Package material manufacturer	KCC	**No. of mask steps**	NA

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Liang Gao	March 2, 2011	Robin Sun	March 2, 2011

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :DDZ43-7 SWR1010080 CUSTOMER: Package:SOD123 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION: Zetex wafer Z4430 qual;1.0Cu wire; KTMC1050G				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VF@IF=10mA Characteristic VZ@IZ=5mA Characteristic ZZT@IZ=5mA Characteristic IR@VR=33V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=34.4V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=34.4V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=34.4V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	
7.3.5.7 (9)	H3TRB	T=85*C RH=85% Vr=34.4v	1	77		
	Pretest		1	77	0/77	
	@ 500Hours	T=85*C RH=85% Vr=34.4v	1	77	0/77	
	Final 1000 Hours	T=85*C RH=85% Vr=34.4v	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=46v/Iz=8mA, PER MIL-STD-750 METHOD 1037				
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8kV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 02/08/11	Approved by:Adam Gu 02/08/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	DMMT5551S-7-F	**Lead material type**	EFTEC-64T
Package Type	SOT-26	**Lead Material manufacturer**	PBE / ASM
DIE P/N	C5983D23H	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-26E
Wafer Diameter	5 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Phenitec	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-Si
Die attach Method / Material	EPOXY	**Front metal thickness (Top layer)**	2.7um
Bond wire material & dia.	Copper Wire, 1.0mil	**Back metal type (All layers)**	Au+As-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	0.9um
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	4	**Die size (width x length x thickness) in mm**	0.44*0.44*0.23
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	9000A SiN
Package material manufacturer	HITACHI	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	November 15, 2012	Bill Tian	November 15, 2012

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: DMMT5551S-7-F SWR1112023 Package: SOT26			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: Phenitec wafer:C5983S 1GCV-6911,1.0 mil Copper wire+CEL-1702HF9 SKF				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	600	0/600	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125, Ta4=150 BVCEO@IC= 10.0mA ICBO @VCB= 64V HFE@VCE= 5V,IC= 1A VCESAT@IC= 1A,IB= 100mA	N/A	N/A		
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vc=144V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vc=144V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150*C Vc=144V, PER JESD22 A-108	1	77	0/77	
7.3.5.4(6)	HIGH TEMP. Storage Life (HTS)	T=150*C , PER JESD22 A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150*C , PER JESD22 A-103	1	45	0/45	
	Final 1000 Hours	T=150*C , PER JESD22 A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=64V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85*C RH=85% Vc=64V	N/A	N/A		
	Final 1000 Hours	T=85*C RH=85% Vc=64V	N/A	N/A		
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130*C RH=85% Vc=42V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130*C RH=85% Vc=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=10mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	N/A	N/A		MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260*C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245*C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A		
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 04/03/12	Approved by: Adam Gu 04/03/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	DN350T05-7	**Lead material type**	Alloy 42
Package Type	SOT-23	**Lead Material manufacturer**	PBE / VAST / APL
DIE P/N	CP956	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-23A
Wafer Diameter	5 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Phenitec	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-Si-Cu
Die attach Method / Material	Eutectic	**Front metal thickness (Top layer)**	2.0um
Bond wire material & dia.	Copper Wire, 1.0mil	**Back metal type (All layers)**	Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	1.2
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.72*0.72*0.23 mm
Package material type	GR640HV-L1	**Die passivation thickness range**	9000A
Package material manufacturer	Henkel	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	March 26, 2013	Bill Tian	March 26, 2013

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: DN350T05 SWR1212036 CUSTOMER: Package: SOT23 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION: Phenitec Wafer:CP956 2GHW-3707,1.0mil Cu wire + GR640HV-L1				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet	1	25	0/25	
	Lot #2	Ta1=25C, Ta2=85C, Ta3=125C, Ta4=150C BVCBO @IC=1mA ICBO @VCB=250V HFE @Vce=10V,Ic=100mA	N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150°C Vc=280V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150°C Vc=280V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150°C Vc=280V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150°C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150°C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150°C , PER JESD22A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55°C-150°C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121°C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85°C RH=85% Vc=64V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85°C RH=85% Vc=64V	N/A	N/A		
	Final 1000 Hours	T=85°C RH=85% Vc=64V	N/A	N/A		Remark1
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130°C RH=85% Vc=42V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130°C RH=85% Vc=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=10mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	N/A	N/A	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260°C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot has passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 06/07/13	Approved by: Adam Gu 06/07/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	DP350T05-7	**Lead material type**	Alloy 42
Package Type	SOT-23	**Lead Material manufacturer**	PBE / VAST / APL
DIE P/N	AP964	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-23A
Wafer Diameter	5 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Phenitec	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-Si-Cu
Die attach Method / Material	Eutectic	**Front metal thickness (Top layer)**	2.0 um
Bond wire material & dia.	Copper Wire, 1.0mil	**Back metal type (All layers)**	Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	0.9 um
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.72*0.72*0.23 mm
Package material type	GR640HV-L1	**Die passivation thickness range**	Yes
Package material manufacturer	Henkel	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	February 22, 2013	Bill Tian	February 22, 2013

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: DP350T05-7 SWR1209208 Package: SOT23			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: Phenitec wafer:AP964 2AHU-8526-01 #45,1.0mil Copper wire				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	385	0/385	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125C, Ta4=150C BVCBO @IC=100uA ICBO @VCB=200V HFE @Vce=10V,Ic=100mA Vcesat @Ic=50mA,Ib=5mA	N/A	25	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150°C Vc=280V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150°C Vc=280V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150°C Vc=280V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150°C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150°C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150°C , PER JESD22A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55°C-150°C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121°C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85°C RH=85% Vc=100V	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=85°C RH=85% Vc=100V	1	77	0/77	
	Final 1000 Hours	T=85°C RH=85% Vc=100V	1	77	0/77	
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130°C RH=85% Vc=42V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130°C RH=85% Vc=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=10mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2min s on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	N/A	N/A	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260°C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245°C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A	0/10	287℃/W
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 01/04/13	Approved by: Susan Ding 01/04/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	DXT5551-13	**Lead material type**	CDA194FH
Package Type	SOT-89	**Lead Material manufacturer**	VAST/XMYH
DIE P/N	C5983S	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT89-3L
Wafer Diameter	5 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Phenitec	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	125 °C/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSiCu
Die attach Method / Material	EPOXY/8200TI	**Front metal thickness (Top layer)**	2.7um
Bond wire material & dia.	Copper Wire,1.0mil	**Back metal type (All layers)**	Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	1.2um
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.44*0.44*0.23mm
Package material type	EME-G600	**Die passivation thickness range**	9000A
Package material manufacturer	SUMITOMO	**No. of mask steps**	5

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	November 17, 2011	Robin Sun	November 17, 2011
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: DXT5551-13 SWR1202070 Package: SOT89-3L			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: Phenitec wafer:C5983S 1GCV-6911,1.0mil Cu wire + EME-G600				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125C, Ta4=150C ICBO @VCB=120V HFE @Vce=5V,Ic=50mA Vcesat @Ic=50mA,Ib=5mA	1	25	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150°C Vc=144V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150°C Vc=144V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150°C Vc=144V, PER JESD22 A-108	1	77	0/77	
7.3.5.4(6)	HIGH TEMP. Storage Life (HTS)	T=150°C , PER JESD22 A-103	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150°C , PER JESD22 A-103	1	77	0/77	
	Final 1000 Hours	T=150°C , PER JESD22 A-103	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55°C-150°C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121°C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85°C RH=85% Vc=100V	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=85°C RH=85% Vc=100V	1	77	0/77	
	Final 1000 Hours	T=85°C RH=85% Vc=100V	1	77	0/77	
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130°C RH=85% Vc1=42V/Vc2=32V,PER JESD22 A-110	N/A	N/A		
	Pretest		N/A	N/A		
	After 96hrs	T=130°C RH=85% Vc=42V/Vc2=32V	N/A	N/A		
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=30mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260°C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245°C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot has passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 01/08/13	Approved by: Adam Gu 01/08/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	DZT3150-13	**Lead material type**	CDA194FH
Package Type	SOT-223	**Lead Material manufacturer**	VAST/XMYH
DIE P/N	C5946S BIN3	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-223B
Wafer Diameter	5 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Phenitec	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	125℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSiCu
Die attach Method / Material	EPOXY/8200TI	**Front metal thickness (Top layer)**	3.0um
Bond wire material & dia.	Copper Wire,1.7 mil	**Back metal type (All layers)**	Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	1.2um
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	3	**Die size (width x length x thickness) in mm**	0.94*0.94*0.23mm
Package material type	EME-G600	**Die passivation thickness range**	9000A
Package material manufacturer	SUMITOMO	**No. of mask steps**	5

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

	Completed by	Date	Certified by	Date
Typed/Printed	Yoyo Tan	November 7, 2012	Bill Tian	November 7, 2012
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: DZT3150-13 SWR1202111 Package: SOT223			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: Phenitec Wafer:C5946S BIN3 1GCY-9049,1.7mil Cu wire + EME-G600				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	600	0/600	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=_____, Ta2=_____, Ta3=_____, Ta4=_____ Characteristic _____ @ ___ = _____ Characteristic _____ @ ___ = _____ Characteristic _____ @ ___ = _____ Characteriatic _____ @ ___ = _____	N/A	N/A		
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vc=40V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vc=40V, PER JESD22 A-108	1	77	0/77	
	Final	T=150*C Vc=40V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150*C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150*C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150*C , PER JESD22A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=40V	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=85*C RH=85% Vc=40V	1	77	0/77	
	Final 1000 Hours	T=85*C RH=85% Vc=40V	1	77	0/77	
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130*C RH=85% Vc=42V,PER JESD22 A-110	N/A	N/A		
	Pretest		N/A	N/A		
	After 96hrs	T=130*C RH=85% Vc=42V	N/A	N/A		
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=15V Ic=60mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	N/A	N/A		
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260*C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245*C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A		
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot has passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 09/25/12	Approved by: Adam Gu 09/25/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Printed specifications are not controlled documents. Verify revision before using.

Assembly and Test Site	DIODES INC	**Glass Transition Temperature (T_G)**	130℃
DIC P/N	FMMT591TA	**Lead Frame Type**	SOT-23F
Package Type	SOT-23	**Lead Frame Manufacturer**	PBE/VAST/APL
DIE P/N	FMMT591T3C	**Lead Frame Material**	Alloy42
Die Line or Process	Transistor	**Terminal Finish (Plating) Material**	Pb free
Wafer Diameter	6 inch	**Header Plating (Die Land Area)**	Silver Spot Plate
Wafer Fab Site(s)	OFAB	**Max Junction Temperature (T_j)**	150℃
ID Method (multiple sites)	N/A	**Max Thermal Resistance Junction to Case (θ_{JC})**	N/A
Assembly Locations(s)	IODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max Thermal Resistance Junction to Ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front Metal Type (Top Layer)**	AlSiCu
Die attach Method / Material	EUTECTIC	**Front Metal Thickness (Top Layer)**	3.0 um
Bond Wire/Clip Material & Wire Diameter	Copper Wire 1.0 mil	**Back Metal Type (All Layers)**	Au
Bond Type (at top side of the die)	Thermo sonic	**Back Metal Thickness (all Layers)**	N/A
Bond Type (at leadframe)	Thermo sonic	**Die Conformal Coating (Passivation)**	N/A
No. of Bonds over Active Area	2	**Die Passivation Thickness Range**	N/A
Mold Compound Material Type	GR640HV-1	**Die Size (Width x Length x Thickness) in mm**	0.686*0.686*0.178mm
Mold Compound Material Manufacturer	Henkel	**No. of Mask Steps**	N/A

Completed by		**Date**	**Certified by**	**Date**
Typed/Printed	Yoyo Tan	July 24, 2013	Bill Tian	July 24, 2013
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: FMMT591TA SWR1303330 Package: SOT23			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: OFAB Wafer:FMMT591T3C 9P38BOGGY.1,Cu 1.0mil + GR640HV-L1				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125C, Ta4=150C BVCBO @IC=-100uA ICBO @VCB=-60V HFE @Vce=-5V,Ic=-500mA Vcesat @Ic=-500mA,Ib=-50mA	1	25	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vc=64V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vc=64V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vc=64V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150*C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150*C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150*C , PER JESD22A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=60V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85*C RH=85% Vc=60V	N/A	N/A		
	Final 1000 Hours	T=85*C RH=85% Vc=60V	N/A	N/A		
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130*C RH=85% Vc=42V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130*C RH=85% Vc=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=10mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2min s on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	4	0/4	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260*C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 06/14/13	Approved by: Adam Gu 06/14/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	135℃
DIC P/N	GDZ4V7LP3-7	**Lead material type**	SLP0603P2-D
Package Type	X3-DFN0603-2	**Lead Material manufacturer**	PBE
DIE P/N	Z9047U	**Lead plating/ coating**	100% Tin / Pb free
Die line or process	ZENER	**Lead frame material type**	EFTEC64
Wafer Diameter	5"	**Header plating (Die land area)**	Selective Ag Plating
Wafer Fab Site(s)	KFAB	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	500 ℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-1%Si
Die attach Method / Material	EUTECTIC	**Front metal thickness (Top layer)**	20kA
Bond wire material & dia.	Copper wire, 0.8MIL	**Back metal type (All layers)**	NiV-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	125A-5150A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	N/A
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	200*200*100um
Package material type	EME-G770HCD	**Die passivation thickness range**	18,000A - 22,000A
Package material manufacturer	SUMITOMO	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Jenny Liu	April 2, 2013	Bill Tian	Apr 2,2013
Signature				
Title				

S

Reliability Test Summary Report

FACTORY: SAT	PART NUMBER :GDZ4V7LP3 SWR1303018 Package:DFN0603-2 DIODES INC.:					
LABORATORY (If Different):	PART DESCRIPTION:KFAB wafer Z9047U/ 0.8Cu qual,					
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VZ@IZT=5mA Characteristic IR@VR=1V Characteristic VF@IF=10mA	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vz=3.7V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vz=3.7V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vz=3.7V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	
7.3.5.7 (9)	HAST	T=130*C RH=85% Vz=3.7v	1	77		
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vz=3.7v	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=4.8v/Iz=23mA, PER MIL-STD-750 METHOD 1037				15000cy @2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560CY	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000CY	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	2	0/2	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 5/29/13	Approved by:Adam Gu 5/29/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110℃
DIC P/N	MMBD3004BRM	**Lead material type**	EFTEC-64
Package Type	SOT-26	**Lead Material manufacturer**	MHT/VAST
DIE P/N	D1089BT/D1089B	**Lead plating/ coating**	Pb free
Die line or process	Planar Process technology	**Lead frame material type**	EFTEC-64
Wafer Diameter	5 inch	**Header plating (Die land area)**	Ag
Wafer Fab Site(s)	Fabtech	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. Diodes Shanghai Co.,Ltd	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	Diodes Shanghai Co.,Ltd	**Front metal type (Top layer)**	AlSi
Die attach Method / Material	Epoxy(9005SP)	**Front metal thickness (Top layer)**	3.5um
Bond wire material & dia.	1.0mil copper wire	**Back metal type (All layers)**	NiV/Au
Bond type (at top side of the die)	Thermo-Ultrasonic	**Back metal thickness (all Layers)**	125A NiV+5150 Au
Bond type (at leadframe)	Epoxy	**Die conforming coating**	Not specified
No. of bonds over active area	4	**Die size (width x length x thickness) in mm**	D1089B: 0.400 x 0.400 x0.216 D1089BT: 0.400 x 0.400 x0.150
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	Not specified
Package material manufacturer	Hitachi Chemical	**No. of mask steps**	5

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Hill Chen	August 16, 2011	Phil Mao	August 16, 2011
Signature				
Title	Wafer Engineer			Wafer Section Manager

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: MMBD3004BRM SWR1203088 CUSTOMER: Package:SOT143 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:KFAB wafer D1089BT top metal change for copper wire conversion qual				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VBR @IR=100uA Characteristic VF @IF=1mA Characteristic VF @IF=10mA Characteristic VF @IF=100mA Characteristic IR @VR=30V Characteristic IR @VR=25V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=240V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=240V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=240V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9)	HAST	T=130*C RH=85% Vr=42V				
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vr=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=225mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	refer to CT data
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000H full hirel test.					
Submitted by:Joan Yu 12/15/12		Approved by:Adam Gu 12/15/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	MMBT2222A-7-03-F	**Lead material type**	CDA194
Package Type	SSOT-23	**Lead Material manufacturer**	PBE / Hitachi
DIE P/N	CP081DE	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT23-R
Wafer Diameter	5 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Phenitec	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	403℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-Si-Cu
Die attach Method / Material	EPOXY	**Front metal thickness (Top layer)**	2.0um
Bond wire material & dia.	Copper Wire, 1.0mil	**Back metal type (All layers)**	Au+As-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	1.2um
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.42*0.42*0.23
Package material type	GR640HV-1	**Die passivation thickness range**	9000A
Package material manufacturer	Henkel	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	November 15, 2012	Bill Tian	November 15, 2012

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: MMBT2222A-7-03-F SWR1111100 CUSTOMER: Package: SOT23 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION: Phenitec wafer:CP081 1GHV-4721,1.0mil Copper wire				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	385	0/385	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125C, Ta4=150C ICBO @VCB=60V HFE @Vce=10V,Ic=10mA Vcesat @Ic=150mA,Ib=15mA	1	25	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150°C Vc=60V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150°C Vc=60V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150°C Vc=60V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150°C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150°C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150°C , PER JESD22A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55°C-150°C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121°C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85°C RH=85% Vc=60V	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=85°C RH=85% Vc=60V	1	77	0/77	
	Final 1000 Hours	T=85°C RH=85% Vc=60V	1	77	0/77	
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130°C RH=85% Vc=42V,PER JESD22 A-110	N/A	N/A		
	Pretest		N/A	N/A		
	After 96hrs	T=130°C RH=85% Vc=42V	N/A	N/A		
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=10mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	N/A	N/A	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260°C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245°C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A	0/10	334℃/W
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot failed on 1000hrs hi-rel test.					
Submitted by:	Sean Huang 04/03/12	Approved by: Susan Ding 04/03/12				

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CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	MMST5401-7-F	**Lead material type**	Alloy 42
Package Type	SOT-323	**Lead Material manufacturer**	PBE
DIE P/N	A5983F	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-323A
Wafer Diameter	5 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Phenitec	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-Si
Die attach Method / Material	Eutectic	**Front metal thickness (Top layer)**	2.7um
Bond wire material & dia.	Copper Wire, 1.0mil	**Back metal type (All layers)**	AuAs-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	0.9 um
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.44*0.44*0.23
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	9000A
Package material manufacturer	HITACHI	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	November 15, 2012	Bill Tian	November 15, 2012

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: MMST5401-7-F SWR1112215 Package: SOT323			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: Phenitec Wafer:A5983F 1GCV-6917,1.0mil Cu wire + CEL-1702HF9 SK				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	600	0/600	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125C, Ta4=150C ICBO @VCB=150V HFE @Vce=5V,Ic=50mA Vcesat @Ic=50mA,Ib=5mA	1	25	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150°C Vc=128V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150°C Vc=128V, PER JESD22 A-108	1	77	0/77	
	Final	T=150°C Vc=128V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150°C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150°C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150°C , PER JESD22A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55°C-150°C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121°C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85°C RH=85% Vc=60V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85°C RH=85% Vc=60V	N/A	N/A		
	Final 1000 Hours	T=85°C RH=85% Vc=60V	N/A	N/A		
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130°C RH=85% Vc=42V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130°C RH=85% Vc=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=20V Ic=10mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2min s on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	N/A	N/A	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260°C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245°C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A	0/10	379℃/W
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 08/01/12	Approved by: Adam Gu 08/01/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	MMST5551-7-F	**Lead material type**	Alloy 42
Package Type	SOT-323	**Lead Material manufacturer**	PBE
DIE P/N	C5983D23H	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-323A
Wafer Diameter	5 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Phenitec	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	625℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-Si
Die attach Method / Material	Eutectic	**Front metal thickness (Top layer)**	2.7um
Bond wire material & dia.	Copper Wire, 1.0mil	**Back metal type (All layers)**	Au+As-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.44*0.44*0.23
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	9000A
Package material manufacturer	HITACHI	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	November 15, 2012	Bill Tian	November 15, 2012

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: MMST5551-7-F SWR1112136 Package: SOT323			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: KFAB wafer: C5983S 1GCV-6912,1.0 mil Cu wire + CEL-1702HF9 SK				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125C, Ta4=150C ICBO @VCB=120V HFE @Vce=5V,Ic=50mA Vcesat @Ic=50mA,Ib=5mA	N/A	N/A	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vc=144V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vc=144V, PER JESD22 A-108	1	77	0/77	
	Final	T=150*C Vc=144V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=60V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85*C RH=85% Vc=60V	N/A	N/A		
	Final 1000 Hours	T=85*C RH=85% Vc=60V	N/A	N/A		
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130*C RH=85% Vc=42V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130*C RH=85% Vc=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=10mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2min s on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	N/A	N/A	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260*C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245*C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 26/03/13	Approved by: Susan Ding 26/03/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130C
DIC P/N	SDM02U30LP3-7B	**Lead material type**	EFTEC64T-1/2H
Package Type	DFN0603H3-2	**Lead Material manufacturer**	DPN
DIE P/N	S0651U	**Lead plating/ coating**	Leadfree
Die line or process	Sky	**Lead frame material type**	SLP0603P2-K DFN0603H3-2
Wafer Diameter	6 inch	**Header plating (Die land area)**	Platting Ag
Wafer Fab Site(s)	KFAB	**Max junction temperature(T_j)**	125C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	500C/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSi1
Die attach Method / Material	Eutectic/N/A	**Front metal thickness (Top layer)**	2um
Bond wire material & dia.	Cu wire, 0.8mil	**Back metal type (All layers)**	NiV+Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NiV (125A) + Au (5150A)
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	SiOx
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.21*0.21*0.10
Package material type	EME-G770HCD	**Die passivation thickness range**	9000A
Package material manufacturer	Sumitomo	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yam Zhang	May 8, 2013	Bill Tian	May 8, 2013
Signature	Yam Zhang	May 8, 2013	Bill Tian	May 8, 2013

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary

FACTORY:SAT		PART NUMBER : SDM02U30LP3 SWR1302058 Package Description : DFN0603H3-2		CUSTOMER: DIODES INC.:		
LABORATORY (If Different):		PART DESCRIPTION : Qual for KFAB wafer: S0651U lot 50114519 #16 (0.8mil Cu + EME-G770HCD).				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-65°C, Ta2=25°C, Ta3=85°C, Ta4=125°C, Ta5=150°C Characteristic VF @ IF = 10mA Characteristic IR @ VR = 10V Characteristic IR @ VR = 30V	1 of 3	25	0/25	
	Lot #2		2 of 3	25	N/A	
	Lot #3		3 of 3	25	N/A	
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150℃ VR=24V, PER JESD22 A-108				
	Pretest		1	77	0/77	
	@ 168 Hours	T=150℃ VR=24V, PER JESD22 A-108	1	77	0/77	
	@ 500 Hours	T=150℃ VR=24V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150℃ VR=24V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	T=150℃ Vg=20V, PER JESD22 A-108				
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65℃-150℃, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 168 Cycles	T=-65℃-150℃, PER JESD22 A-104	1	77	0/77	
	@ 500 Cycles	T=-65℃-150℃, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65℃-150℃, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121℃ 15PSIG 100%RH				96hrs
	Pretest		1	77	0/77	
	Final 96 Hours	T=121℃ 15PSIG 100%RH	1	77	0/77	
7.3.5.7 (9-1)	Highly Accelerated Stress Test(HAST)	T=130℃ RH=85% VR=24V				96hrs
	Pretest		1	77	0/77	
	Final 96 Hours	T=130℃ RH=85% VR=24V	1	77	0/77	
7.3.5.7 (9-2)	High Humidity High Temp. Reverse Bias(H^3TRB)	T=85℃ RH=85% Vd=24V	1	77	N/A	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	IF=200mA; PER MIL-STD-750 METHOD 1037				15000cyc 2mins on/off
	Pretest		1	77	0/77	
	@ 2520 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	@ 7560 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	Final 15000 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77	N/A	
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 MM 0/10 HBM	200V 4kV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30	N/A	
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30	N/A	
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260℃@30sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245℃@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	Rthjc 286°C/W
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	30	0/30	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	30	0/30	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	30	0/30	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS)	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary: The lot passed the precondition test and 1000hrs hi-rel tests.						
Submitted by: Joan Yu 09/21/13		**Approved by: Adam Gu 09/20/13**				

Q-Form Q014-4,Rev.K

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	140℃
DIC P/N	TPD6V8LP-7	**Lead material type**	SLP1006P2
Package Type	DFN1006-2	**Lead Material manufacturer**	MHT
DIE P/N	Z5068Q	**Lead plating/ coating**	Ni/Pd/Au
Die line or process	Planar process technology	**Lead frame material type**	Copper
Wafer Diameter	5inch	**Header plating (Die land area)**	Copper
Wafer Fab Site(s)	FabTech	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. Diodes Shanghai Co.,Ltd	**Max thermal resistance junction to ambient (θ_{JA})***	500°C/W
Test Locations(s)	Diodes Shanghai Co.,Ltd	**Front metal type (Top layer)**	Mo-Al-1%Si
Die attach Method / Material	EPOXY QMI519	**Front metal thickness (Top layer)**	2.3KÅ Mo – 20KÅ Al-Si
Bond wire material & dia.	Cu Wire 0.8mil	**Back metal type (All layers)**	Au-Si Eutectic
Bond type (at top side of the die)	Thermo-Ultrasonic	**Back metal thickness (all Layers)**	1.2µm Au – Alloyed w/Si
Bond type (at leadframe)	Thermo-Ultrasonic	**Die conforming coating**	N/A
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.35 x 0.35 x 0.14
Package material type	EME-G770HCD	**Die passivation thickness range**	6KÅ - 9KÅ
Package material manufacturer	SUMITOMO	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Charlie Tang	May 27, 2011		May 27, 2011
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :TPD6V8LP SWR1104220 SWR1106301 SWR1106300 CUSTOMER: Package:DFN1006-2 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:FT wafer Z5068Q/50092974 qual;1.0Cu wire; EME-G770HCD				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	312	0/312	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VZ@IZ=5mA Characteristic ZZT@IZ=5mA Characteristic ZZK@IZ=0.5mA Characteristic IR@VR=2.5	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C VZ=5.4V, PER JESD22 A-108	1	78		
	Pretest		1	78	0/78	
	@ 500 Hours	T=150*C VZ=5.4V, PER JESD22 A-108	1	78	0/78	
	Final 1000Hours	T=150*C VZ=5.4V, PER JESD22 A-108	1	78	0/78	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	78	0/78	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	78	0/78	96H
7.3.5.7 (9)	H3TRB	T=85*C RH=85% VZ=5.4v	1	78		
	Pretest		1	78	0/78	
	@ 500Hours	T=85*C RH=85% VZ=5.4v	1	78	0/78	
	Final 1000 Hours	T=85*C RH=85% VZ=5.4v	1	78	0/78	
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vr=5.4v	1	78	0/78	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=7V/Iz=35mA, PER MIL-STD-750 METHOD 1037				
	Pretest	MIL-STD-750 METHOD 1037	1	78	0/78	
	Midpoint	MIL-STD-750 METHOD 1037	1	78	0/78	
	After	MIL-STD-750 METHOD 1037	1	78	0/78	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	MM 400V HBM 8kV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/60	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 8/18/11	Approved by:Adam Gu 8/18/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	UDZ5V6B-7	**Lead material type**	Alloy 42
Package Type	SOD-323	**Lead Material manufacturer**	MHT,VAST,NBKQ,XMYH
DIE P/N	Z1056	**Lead plating/ coating**	Pb free
Die line or process	Zener	**Lead frame material type**	Alloy 42
Wafer Diameter	5inch	**Header plating (Die land area)**	NA
Wafer Fab Site(s)	DFT	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A ℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-1%Si
Die attach Method / Material	EUTECTIC	**Front metal thickness (Top layer)**	2um
Bond wire material & dia.	Copper Wire, 1.0mil	**Back metal type (All layers)**	Ti-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.28*0.28*0.216mm
Package material type	KTMC1050G	**Die passivation thickness range**	NA
Package material manufacturer	KCC	**No. of mask steps**	NA

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Liang Gao	March 2, 2011	Robin Sun	March 2, 2011

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :UDZ5V6B-7 SWR1010083 CUSTOMER: Package:SOD323 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION: Zetex wafer Z1056 qual;1.0Cu wire; KTMC1050G				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VZ@IZ=5mA Characteristic ZZT@IZ=5mA Characteristic ZZK@IZ=0.5mA Characteristic IR@VR=2.5	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=4.5V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vr=4.5V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=4.5V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	
7.3.5.7 (9)	H3TRB	T=85*C RH=85% Vr=4.5v	1	77		
	Pretest		1	77	0/77	
	@ 500Hours	T=85*C RH=85% Vr=4.5v	1	77	0/77	
	Final 1000 Hours	T=85*C RH=85% Vr=4.5v	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=5.7v/Iz=35mA, PER MIL-STD-750 METHOD 1037				
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8kV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 02/17/11	Approved by:Adam Gu 02/17/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110℃
DIC P/N	UDZ7V5B-7-01	**Lead material type**	Alloy42
Package Type	SOD-323	**Lead Material manufacturer**	VAST/MHT/XMYH/NBKQ
DIE P/N	Z1075	**Lead plating/ coating**	Pb free
Die line or process	ZENER	**Lead frame material type**	Alloy42
Wafer Diameter	5"	**Header plating (Die land area)**	Spot Ag
Wafer Fab Site(s)	FABTECH	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	NA	**Max thermal resistance junction to case (θ_{JC})**	NA
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	NA
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-1%Si
Die attach Method / Material	EUTECTIC	**Front metal thickness (Top layer)**	20KA
Bond wire material & dia.	Cu wire, 1.0MIL	**Back metal type (All layers)**	NiV-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	125A-5150A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.28*0.28*0.216mm
Package material type	*KTMC1050G	**Die passivation thickness range**	6,000A - 9,000A
Package material manufacturer	KCC	**No. of mask steps**	4

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Helen Wang	May 25, 2011	Robin Sun	May 25, 2011
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER :UDZ7V5B-7-01 SWR1104239/SWR1105301/SWR1105302 CUSTOMER: Package:SOD323 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION: FT wafer Z1075,1.0 copper wire qual; KTMC1050G				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	312	0/312	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VZ@IZ=5mA Characteristic ZZT@IZ=5mA Characteristic ZZK@IZ=0.5mA Characteristic IR@VR=2.5	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=6V, PER JESD22 A-108	1	78		
	Pretest		1	78	0/78	
	@ 500 Hours	T=150*C Vr=6V, PER JESD22 A-108	1	78	0/78	
	Final 1000Hours	T=150*C Vr=6V, PER JESD22 A-108	1	78	0/78	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066			N/A	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	78	0/78	
	@ 500 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	78	0/78	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	78	0/78	96H
7.3.5.7 (9)	H3TRB	T=85*C RH=85% Vz=6v	1	78		
	Pretest		1	78	0/78	
	@ 500Hours	T=85*C RH=85% Vz=6v	1	78	0/78	
	Final 1000 Hours	T=85*C RH=85% Vz=6v	1	78	0/78	
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vz=6v	1	78	0/78	96H
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vz=7.7v/Iz=26mA, PER MIL-STD-750 METHOD 1037				15000cycles @2 min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	78	0/78	
	Midpoint	MIL-STD-750 METHOD 1037	1	78	0/78	
	After	MIL-STD-750 METHOD 1037	1	78	0/78	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	78		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	78		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	78		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	78		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	25	0/25	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
Summary:	The lot passed 1000hrs full hi-rel test.					
Submitted by:	Joan Yu 8/12/11	Approved by:Adam Gu 8/12/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	160C
DIC P/N	ZLLS1000TA	**Lead material type**	CDA194
Package Type	SSOT-23	**Lead Material manufacturer**	MHT/VAST/PBE
DIE P/N	S0342D	**Lead plating/ coating**	Etching
Die line or process	SKY	**Lead frame material type**	SOT-23R
Wafer Diameter	5inch	**Header plating (Die land area)**	Spot Plating
Wafer Fab Site(s)	KFAB	**Max junction temperature(T_j)**	125C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al
Die attach Method / Material	N/A	**Front metal thickness (Top layer)**	N/A
Bond wire material & dia.	Cu wire, 1.0mil	**Back metal type (All layers)**	TiAu
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	N/A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	N/A
No. of bonds over active area	3	**Die size (width x length x thickness) in mm**	0.88*0.88*0.2
Package material type	KTMC1050G	**Die passivation thickness range**	N/A
Package material manufacturer	KCC	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Caixia Wei	September 16, 2011	Robin Sun	Sep 16, 2011
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: ZLLS1000TA SWR1211303 CUSTOMER: Package:SOT23 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Copper wire 1.0mil,KFAB wafer S0342D, KTMC1050G				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VBR @IR=500uA Characteristic VF @IF=1A Characteristic VF @IF=1.5A Characteristic IR @VR=40V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=32V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 168 Hours	T=150*C Vr=32V, PER JESD22 A-108	1	77	0/77	
	@ 500 Hours	T=150*C Vr=32V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=32V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vr=32V	1	77		
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vr=32V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=1A; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	After	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	2	0/2	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 03/15/13		Approved by:Adam Gu 03/15/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	120C
DIC P/N	ZLLS2000TA	**Lead material type**	EFTEC-64T
Package Type	SOT-26	**Lead Material manufacturer**	MHT/VAST/XMYH/NBKQ
DIE P/N	S0364D	**Lead plating/ coating**	Stamping
Die line or process	SKY	**Lead frame material type**	SOT-26C
Wafer Diameter	5inch	**Header plating (Die land area)**	Spot Plating
Wafer Fab Site(s)	KFAB	**Max junction temperature(T_j)**	150C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSi
Die attach Method / Material	N/A	**Front metal thickness (Top layer)**	4 um
Bond wire material & dia.	Cu wire, 1.7mil	**Back metal type (All layers)**	TiAu
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	N/A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	N/A
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	1.83*0.96*0.2
Package material type	CEL-1702HF9 SK	**Die passivation thickness range**	N/A
Package material manufacturer	HITACHI	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Caixia Wei	September 16, 2011	Robin Sun	Sep 16, 2011
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: ZLLS2000TA SWR1211299 CUSTOMER: Package:SOT26 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Copper wire 1.7mil,KFAB wafer S0364D,CEL-1702HF9.SK.				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VBR @IR=1mA Characteristic VF @IF=1A Characteristic VF @IF=1.5A Characteristic VF @IF=2A Characteristic VF @IF=3A Characteristic IR @VR=30V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=32V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 168 Hours	T=150*C Vr=32V, PER JESD22 A-108	1	77	0/77	
	@ 500 Hours	T=150*C Vr=32V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=32V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vr=32V	1	77		
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vr=32V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=2A; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10	MM 400V
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	2	0/2	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 03/21/13		Approved by:Adam Gu 03/21/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	160C
DIC P/N	ZLLS410TA	**Lead material type**	Alloy 42
Package Type	SOD-323	**Lead Material manufacturer**	MHT/VAST/XMYH/NBKQ
DIE P/N	S4433D	**Lead plating/ coating**	Pure Sn
Die line or process	Sky	**Lead frame material type**	Alloy 42
Wafer Diameter	5 inch	**Header plating (Die land area)**	Spot Ag
Wafer Fab Site(s)	KFAB	**Max junction temperature(T_j)**	150C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Ti-Al/1%Si
Die attach Method / Material	Epoxy(8200TI)	**Front metal thickness (Top layer)**	1100A Ti, 40kA AlSi
Bond wire material & dia.	Cu wire, 1.7mil	**Back metal type (All layers)**	Ti-NiV-Au
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	1500A Ti, 3300A NiV, 1200A Au
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	N/A
No. of bonds over active area	1	**Die size (width x length x thickness) in mm**	0.71*0.71*0.235
Package material type	KTMC1050G	**Die passivation thickness range**	N/A
Package material manufacturer	KCC	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Caixia Wei	April 23, 2012	Bill Tian	April 23, 2012
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary Report

FACTORY:		PART NUMBER: ZLLS410TA SWR1211298 CUSTOMER: Package:SOD323 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION:Copper wire 1.7mil,KFAB S4433D KTMC1050G				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				N/A
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic VBR @IR=200uA Characteristic VF @IF=1A Characteristic VF @IF=100mA Characteristic IR @VR=10V	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	0/45	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vr=8V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 168 Hours	T=150*C Vr=8V, PER JESD22 A-108	1	77	0/77	
	@ 500 Hours	T=150*C Vr=8V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vr=8V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	MIL-750D, Method 4066	N/A	N/A		N/A
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-65*C-150*C, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-65*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96h
7.3.5.7 (9a)	HAST	T=130*C RH=85% Vr=8V	1	77		
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vr=8V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	If=500mA; PER MIL-STD-750 METHOD 1037				15000Cycles @ 2min on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cy	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cy	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77		N/A
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	1	77		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10	MM 400V
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	2	0/2	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30		N/A
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		N/A
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		N/A
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		N/A
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		N/A
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	30	0/30	260*C @30S
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245*C @5S
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		N/A
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		N/A
Summary:	The lot passed pre-con and 1000hrs full hi-rel test.					
Submitted by:Joan Yu 02/26/13		Approved by:Adam Gu 02/26/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110°C
DIC P/N	ZVN4525E6	**Lead material type**	EFTEC64T
Package Type	SOT23-6	**Lead Material manufacturer**	Mitsui High - Tec [Shanghai] Co Ltd
DIE P/N	ZVN4525GT3D	**Lead plating/ coating**	Pb free
Die line or process	MOSFET	**Lead frame material type**	SOT26C
Wafer Diameter	6inch	**Header plating (Die land area)**	Ag. 3.0 - 8.0um
Wafer Fab Site(s)	OFAB	**Max junction temperature(T_j)**	150°C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	113°C/W For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSi1Cu0.5
Die attach Method / Material	8200TI Epoxy	**Front metal thickness (Top layer)**	3.0um
Bond wire material & dia.	Copper wire, 1.0mil	**Back metal type (All layers)**	Ti/Ni/Ag
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	N/A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	Ox/Nitride
No. of bonds over active area	2 wires	**Die size (width x length x thickness) in mm**	0.9652*1.2954*0.279mm
Package material type	CEL-1702HF9 SK	**Die passivation thickness range**	N/A
Package material manufacturer	Hitachi Chemical [Suzhou]	**No. of mask steps**	7

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Christiana Bob-Manuel	January 17, 2013	Darren Reynold	January 17, 2013
Signature				

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Internet: http://www.diodes.com

Diodes Zetex Semiconductors Limited
ISO/TS16949:2009
FILE NO. 417076

Date: 30/01/2013

Reliability Test Summary

RTS No: 1820

Device Family: VMOS in SOT23-6 (includes ZVN4525E6).
Package: SOT23-6
Date From: 29/05/2012
Date To: 06/11/2012

Environmental Trial Data

Trial Type	Specification	Lots	Devices Tested	Devices Failed	Cumulative Hours	% Failures
DPA (Destructive Physical Analysis)	AEC-Q101-004	1	4	0	4	0.000
EXT VIS (External Visual)	JESD22-B101	1	669	0	754	0.000
HAST (Highly Accelerated Stress Test)	JESD22-A110	1	77	0	7392	0.000
HS (Hot Store)	JESD22-A103	1	45	0	45360	0.000
PCLV (Pre-conditioned Autoclave)	JESD22-A102	1	77	0	7392	0.000
PIOL (Pre-conditioned Intermittent Operating Life)	MIL-STD-750 Method 1037	1	77	0	77616	0.000
PTC (Pre-conditioned Temperature Cycle Air to Air)	JESD22-A104	1	77	0	77616	0.000
PTHB (Pre-conditioned Temperature Humidity + Bias)	JESD22-A101	1	77	0	77616	0.000
RSHD (Resistance to Solder Heat Dip)	JESD22-B106	1	45	0	45	0.000

Electrical Stress Trials

Electrical Trial Type:	**HTRB (High Temperature Reverse Bias - JESD22-A108)**
Service Operating Temperature (°C):	55
Ambient Temperature (°C):	150
Activation Energy (eV):	0.7
Confidence Level (%):	60
Actual Device Hours	77616
Equivalent Device Hours	2.017E+07
Lots	1
Devices Tested:	77
Devices Failed:	0
Mean Time To Failure (Hours):	2.202E+07
Failure Rate FITs:	45.4222
Failure Rate %/1000 Hours:	4.542E-03

Electrical Trial Type:	**HTGB (High Temperature Gate Bias - JESD22-A108)**
Service Operating Temperature (°C):	55
Ambient Temperature (°C):	150
Activation Energy (eV):	0.7
Confidence Level (%):	60
Actual Device Hours	77616
Equivalent Device Hours	2.017E+07
Lots	1

Diodes Zetex Semiconductors Limited
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Internet: http://www.diodes.com

Diodes Zetex Semiconductors Limited
ISO/TS16949:2009
FILE NO. 417076

Number of Devices Tested:	77
Number of Devices Failed:	0
Mean Time To Failure (Hours):	2.202E+07
Failure Rate FITs:	45.4222
Failure Rate %/1000 Hours:	4.542E-03

Christiana Bob-Manuel
Reliability Engineer
Diodes Zetex Semiconductors Limited

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	135°C
DIC P/N	ZVN4525G	**Lead material type**	CDA194FH
Package Type	SOT223	**Lead Material manufacturer**	JIH LIN Technology Co Ltd
DIE P/N	ZVN4525GT3D	**Lead plating/ coating**	Pb free
Die line or process	MOSFET	**Lead frame material type**	SOT-223A
Wafer Diameter	6inch	**Header plating (Die land area)**	Ag. 3.0 - 8.0um
Wafer Fab Site(s)	OFAB	**Max junction temperature(T_j)**	150°C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	63°C/W For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSi1Cu0.5
Die attach Method / Material	Soft-Solder	**Front metal thickness (Top layer)**	3.0um
Bond wire material & dia.	Copper wire, 1.0mil	**Back metal type (All layers)**	Ti/Ni/Ag
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	N/A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	Ox/Nitride
No. of bonds over active area	2 wires	**Die size (width x length x thickness) in mm**	0.9652*1.2954*0.279mm
Package material type	EME-G600	**Die passivation thickness range**	N/A
Package material manufacturer	Sumitomo Bakelite	**No. of mask steps**	7

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Christiana Bob-Manuel	January 17, 2013	Darren Reynold	January 17, 2013
Signature				

Diodes Zetex Semiconductors Limited
Zetex Technology Park, Chadderton,
Oldham, OL9 9LL, United Kingdom.

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E-mail: christiana_bob-manuel@eu.diodes.com
Internet: http://www.diodes.com

Diodes Zetex Semiconductors Limited
ISO/TS16949:2009
FILE NO. 417076

Date: 30/01/2013

Reliability Test Summary

RTS No: 1821

Device Family: VMOS in SOT223 (includes ZVN4525G).
Package: SOT223
Date From: 11/09/2012
Date To: 06/11/2012

Environmental Trial Data

Trial Type	Specification	Lots	Devices Tested	Devices Failed	Cumulative Hours	% Failures
DPA (Destructive Physical Analysis)	AEC-Q101-004	1	4	0	4	0.000
EXT VIS (External Visual)	JESD22-B101	1	669	0	693	0.000
HAST (Highly Accelerated Stress Test)	JESD22-A110	1	77	0	7392	0.000
HS (Hot Store)	JESD22-A103	1	45	0	45360	0.000
PCLV (Pre-conditioned Autoclave)	JESD22-A102	1	77	0	7392	0.000
PIOL (Pre-conditioned Intermittent Operating Life)	MIL-STD-750 Method 1037	1	77	0	77616	0.000
PTC (Pre-conditioned Temperature Cycle Air to Air)	JESD22-A104	1	77	0	77616	0.000
PTHB (Pre-conditioned Temperature Humidity + Bias)	JESD22-A101	1	77	0	77616	0.000
RSHD (Resistance to Solder Heat Dip)	JESD22-B106	1	45	0	45	0.000

Electrical Stress Trials

Electrical Trial Type:	**HTRB (High Temperature Reverse Bias - JESD22-A108)**
Service Operating Temperature (°C):	55
Ambient Temperature (°C):	150
Activation Energy (eV):	0.7
Confidence Level (%):	60
Actual Device Hours	77616
Equivalent Device Hours	2.017E+07
Lots	1
Devices Tested:	77
Devices Failed:	0
Mean Time To Failure (Hours):	2.202E+07
Failure Rate FITs:	45.4222
Failure Rate %/1000 Hours:	4.542E-03
Electrical Trial Type:	**HTGB (High Temperature Gate Bias - JESD22-A108)**
Service Operating Temperature (°C):	55
Ambient Temperature (°C):	150
Activation Energy (eV):	0.7
Confidence Level (%):	60
Actual Device Hours	77616
Equivalent Device Hours	2.017E+07

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E-mail: christiana_bob-manuel@eu.diodes.com
Internet: http://www.diodes.com

Diodes Zetex
Semiconductors Limited
ISO/TS16949:2009
FILE NO. 417076

Lots	1
Number of Devices Tested:	77
Number of Devices Failed:	0
Mean Time To Failure (Hours):	2.202E+07
Failure Rate FITs:	45.4222
Failure Rate %/1000 Hours:	4.542E-03

Christiana Bob-Manuel
Reliability Engineer
Diodes Zetex Semiconductors Limited

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	ZX5T955GTA	**Lead material type**	CDA194FH
Package Type	SOT-223	**Lead Material manufacturer**	VAST/XMYH
DIE P/N	ZX5T955D	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	Stamping
Wafer Diameter	6 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Ofab	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSi
Die attach Method / Material	SOFT-SOLDER/Pb92.5Sn5Ag2.5	**Front metal thickness (Top layer)**	6.0 um
Bond wire material & dia.	Copper Wire,1.7 mil	**Back metal type (All layers)**	Ti/Ni/Ag
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	3	**Die size (width x length x thickness) in mm**	1.676*1.676*0.229mm
Package material type	EME-G600	**Die passivation thickness range**	N/A
Package material manufacturer	SUMITOMO	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	August 30, 2012	Bill Tian	August 30, 2012
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: ZX5T955GTA SWR1111222 Package: SOT223			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: Zetex wafer:ZX5T955D 9P40UNLED.3,1.7mil Copper wire+EME-G600				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	600	0/600	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125, Ta4=150 BVCEO@IC= 10.0mA ICBO @VCB= 64V HFE@VCE= 5V,IC= 1A VCESAT@IC= 1A,IB= 100mA	N/A	N/A		
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vc=144V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vc=144V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150*C Vc=144V, PER JESD22 A-108	1	77	0/77	
7.3.5.4(6)	HIGH TEMP. Storage Life (HTS)	T=150*C , PER JESD22 A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150*C , PER JESD22 A-103	1	45	0/45	
	Final 1000 Hours	T=150*C , PER JESD22 A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=64V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85*C RH=85% Vc=64V	N/A	N/A		
	Final 1000 Hours	T=85*C RH=85% Vc=64V	N/A	N/A		
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130*C RH=85% Vc=42V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130*C RH=85% Vc=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=30mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	N/A	N/A		MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260*C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245*C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A		
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 04/10/12	Approved by: Adam Gu 04/10/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	ZX5T955GTA	**Lead material type**	CDA 194
Package Type	SOT-223	**Lead Material manufacturer**	VAST/XMYH
DIE P/N	CY955D	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-223A
Wafer Diameter	6 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Kfab	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	150℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSiCu
Die attach Method / Material	SOFT-SOLDER/Pb92.5Sn5Ag2.5	**Front metal thickness (Top layer)**	6um
Bond wire material & dia.	Copper Wire,1.7 mil	**Back metal type (All layers)**	Ti/Ni/Ag
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	3	**Die size (width x length x thickness) in mm**	1.295*1.295*0.229mm
Package material type	EME-G600	**Die passivation thickness range**	N/A
Package material manufacturer	SUMITOMO	**No. of mask steps**	6

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	February 22, 2013	Bill Tian	February 22, 2013
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: ZX5T955GTA SWR1110242 Package: SOT223			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: KFAB wafer:CY955D 50102585,1.7mil Copper wire+EME-G600				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	600	0/600	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125, Ta4=150 BVCEO@IC= 10.0mA ICBO @VCB= 64V HFE@VCE= 5V,IC= 1A VCESAT@IC= 1A,IB= 100mA	N/A	N/A		
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150°C Vc=144V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150°C Vc=144V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150°C Vc=144V, PER JESD22 A-108	1	77	0/77	
7.3.5.4(6)	HIGH TEMP. Storage Life (HTS)	T=150°C , PER JESD22 A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150°C , PER JESD22 A-103	1	45	0/45	
	Final 1000 Hours	T=150°C , PER JESD22 A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55°C-150°C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121°C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85°C RH=85% Vc=48V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85°C RH=85% Vc=48V	N/A	N/A		
	Final 1000 Hours	T=85°C RH=85% Vc=48V	N/A	N/A		
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130°C RH=85% Vc=42V,PER JESD22 A-110	1	77	0/77	
	Pretest		1	77	0/77	
	After 96hrs	T=130°C RH=85% Vc=42V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=30mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	4	0/4	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260°C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245°C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A		
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 03/29/12	Approved by: Adam Gu 03/29/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130°C
DIC P/N	ZXMC4A16DN8TA/ZXMC4A16DN8TC	**Lead material type**	CDA194FH
Package Type	SO-8	**Lead Material manufacturer**	ASM,PBE,NBKQ
DIE P/N	ZXMN4A06T3D + ZXMP4A16T3D	**Lead plating/ coating**	Pb free
Die line or process	MOSFET Trench	**Lead frame material type**	SOIC-8D
Wafer Diameter	150mm	**Header plating (Die land area)**	Ag Spot Plate
Wafer Fab Site(s)	OFAB	**Max junction temperature(T_j)**	150°C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	100 °C/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSiCu0.5
Die attach Method / Material	EPOXY/8200TI	**Front metal thickness (Top layer)**	3.0 um
Bond wire material & dia.	Copper wire, 1.7mil	**Back metal type (All layers)**	Ti/Ni/Ag
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	N/A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	Oxide
No. of bonds over active area	Gate: 1 wire/Die; Source: 4 wires/Die	**Die size (width x length x thickness) in mm**	ZXMN4A06D:1.31*1.71*0.229mm ZXMP4A16D:1.71*1.71*0.229mm
Package material type	EME-G600FL	**Die passivation thickness range**	N/A
Package material manufacturer	SUMITOMO	**No. of mask steps**	ZXMN4A06T3D: 7 layers ZXMP4A16T3D: 5 layers

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Cora Fernando	June 13, 2013		
Signature				

Diodes Zetex Semiconductors Limited
Zetex Technology Park, Chadderton,
Oldham, OL9 9LL, United Kingdom.

Telephone No.: +44 (0)161 622 4444
Direct Tel. No.: +44 (0)161 622 4841
E-mail: christiana_bob-manuel@eu.diodes.com
Internet: http://www.diodes.com

Diodes Zetex Semiconductors Limited
ISO/TS16949:2009
FILE NO. 417076

Date: 30/01/2013

Reliability Test Summary

RTS No: 1819

Device Family: Qualification of Copper Wire Bonding and change of top metal to 3um AlSiCu0.5 of UMOS die assembled at SKE-DSH
Package: SO-8
Date From: 28/02/2012
Date To: 11/09/2012

Environmental Trial Data

Trial Type	Specification	Lots	Devices Tested	Devices Failed	Cumulative Hours	% Failures
DPA (Destructive Physical Analysis)	AEC-Q101-004	2	8	0	8	0.000
EXT VIS (External Visual)	JESD22-B101	3	1279	0	1279	0.000
HAST (Highly Accelerated Stress Test)	JESD22-A110	2	154	0	14784	0.000
HS (Hot Store)	JESD22-A103	2	90	0	90720	0.000
PCLV (Pre-conditioned Autoclave)	JESD22-A102	2	154	0	14784	0.000
PIOL (Pre-conditioned Intermittent Operating Life)	MIL-STD-750 Method 1037	1	77	0	77616	0.000
PTC (Pre-conditioned Temperature Cycle Air to Air)	JESD22-A104	2	154	0	155232	0.000
PTHB (Pre-conditioned Temperature Humidity + Bias)	JESD22-A101	2	154	0	155232	0.000
RSHD (Resistance to Solder Heat Dip)	JESD22-B106	2	90	0	90	0.000

Electrical Stress Trials

Electrical Trial Type: **HTRB (High Temperature Reverse Bias - JESD22-A108)**
Service Operating Temperature (°C): 55
Ambient Temperature (°C): 150
Activation Energy (eV): 0.7
Confidence Level (%): 60

Actual Device Hours 155232
Equivalent Device Hours 4.035E+07
Lots 2
Devices Tested: 154
Devices Failed: 0

Mean Time To Failure (Hours): 4.403E+07
Failure Rate FITs: 22.7111
Failure Rate %/1000 Hours: 2.271E-03

Electrical Trial Type: **HTGB (High Temperature Gate Bias - JESD22-A108)**
Service Operating Temperature (°C): 55
Ambient Temperature (°C): 150
Activation Energy (eV): 0.7
Confidence Level (%): 60

Actual Device Hours 155232
Equivalent Device Hours 4.035E+07

Diodes Zetex Semiconductors Limited
Zetex Technology Park, Chadderton,
Oldham, OL9 9LL, United Kingdom.

Telephone No.: +44 (0)161 622 4444
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Internet: http://www.diodes.com

Diodes Zetex
Semiconductors Limited
ISO/TS16949:2009
FILE NO. 417076

Lots	2
Number of Devices Tested:	154
Number of Devices Failed:	0
Mean Time To Failure (Hours):	4.403E+07
Failure Rate FITs:	22.7111
Failure Rate %/1000 Hours:	2.271E-03

Christiana Bob-Manuel
Reliability Engineer
Diodes Zetex Semiconductors Limited

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110C
DIC P/N	ZXMN10B08E6	**Lead material type**	EFTEC-64T
Package Type	SOT-26	**Lead Material manufacturer**	MHT
DIE P/N	ZXMN10B08T3D	**Lead plating/ coating**	Pb free
Die line or process	MOSFET	**Lead frame material type**	SOT-26C
Wafer Diameter	6 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	OFAB	**Max junction temperature(T_j)**	150C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	113 °C/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSiCu
Die attach Method / Material	Epoxy/8200TI	**Front metal thickness (Top layer)**	3.0 um
Bond wire material & dia.	Copper wire, 1.7mil	**Back metal type (All layers)**	TiNiAg
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	N/A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	N/A
No. of bonds over active area	Gate: 1 wire; Source:4 wires	**Die size (width x length x thickness) in mm**	1.02*1.77*0.229mm
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	N/A
Package material manufacturer	HITACHI	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Robert Shen	November 22, 2012	Bill Tian	November 22, 2012
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary

FACTORY:	PART NUMBER : ZXMN10B08E6 SWR1203178 Package Description : SOT-26	CUSTOMER: DIODES INC.:
LABORATORY (If Different):	PART DESCRIPTION : Qualification for Copper Wire Bonding (wafer: 9ZXMN10B08T -CD, 1.7 Cu wire+ CEL-1702HF9 SK).	

DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	385	0/385	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55℃, Ta2=25℃, Ta3=85℃, Ta4=150℃ Characteristic BVDSS@VGS=0V, ID=250uA Characteristic IDSS@VDS=100V, VGS=0V Characteristic IGSS@VGS=±20V, VDS=0V Characteristic VGS(th)@VDS=VGS, ID=250uA Characteristic RDSON@VGS=10V, ID=1.6A Characteristic RDSON@VGS=4.5V, ID=1.4A Characteristic RDSON@VGS=4.3V, ID=1.1A Characteristic yFS@VDS=15V,ID=1.6A Characteristic VSD@VGS=0V,IS=2.0A	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	N/A	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150℃ Vd=100V, PER JESD22 A-108				
	Pretest		1	77	0/77	
	@ 500 Hours	T=150℃ Vd=100V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150℃ Vd=100V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	T=150℃ Vg=20V, PER JESD22 A-108				
	Pretest		1	77	0/77	
	@ 500 Hours	T=150℃ Vg=20V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150℃ Vg=20V, PER JESD22 A-108	1	77	0/77	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55℃-150℃, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55℃-150℃, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55℃-150℃, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121℃ 15PSIG 100%RH				
	Pretest		1	77	0/77	
	Final 96 Hours	T=121℃ 15PSIG 100%RH	1	77	0/77	
7.3.5.7 (9-1)	Highly Accelerated Stress Test(HAST)	T=130℃ RH=85% Vd=42V	1	77		
	Pretest		1	77	0/77	
	Final 96 Hours	T=130℃ RH=85% Vd=42V	1	77	0/77	
7.3.5.7 (9-2)	High Humidity High Temp. Reverse Bias(H^3TRB)	T=85℃ RH=85% Vd=100V	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=85℃ RH=85% Vd=100V	1	77	0/77	
	Final 1000 Hours	T=85℃ RH=85% Vd=100V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vd=5V / Id=200mA; PER MIL-STD-750 METHOD 1037				2mins on/off
	Pretest		1	77	0/77	
	@ 7560 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	Final 15000 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77	N/A	
7.3.5.9 (11)	High Temperature Storage Life (HTSL)	T=150℃, PER JESD22 A-103				
	Pretest		1	45	0/45	
	@ 500 hours	T=150℃, PER JESD22 A-103	1	45	0/45	
	Final 1000 hours	T=150℃, PER JESD22 A-103	1	45	0/45	
7.3.5.9 (12)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	pass	MM=100V HBM=500V
7.3.5.10 (13)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	4	0/4	
7.3.5.11 (14)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (15)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30	N/A	
7.3.5.13 (16)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30	N/A	
(17)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(20)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (21)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260℃@30sec
7.3.5.15 (22)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245℃@5sec
7.3.5.16 (23)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (24)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (25)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (26)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(27)	UNCLAMPED INDUCTIVE SWITCHING (UIS)	N/A, not for Diode	N/A	N/A		
(28)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		

Summary: The lot passed the precondition test and 1000hrs hi-rel tests.

Submitted by: Jianhua Yang 7/20/12 **Approved by: Adam Gu 7/20/12**

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	135C
DIC P/N	ZXMN6A11Z	**Lead material type**	CDA194HH
Package Type	SOT89	**Lead Material manufacturer**	Suzhou Hitachi Cable Precision Dongguan Possehl Seg Electronics
DIE P/N	ZXMN6A11T3D	**Lead plating/ coating**	Pb free
Die line or process	MOSFET	**Lead frame material type**	SOT89-3L
Wafer Diameter	6 inch	**Header plating (Die land area)**	Ag: 3 - 8um
Wafer Fab Site(s)	OFAB	**Max junction temperature(T_j)**	150°C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	a) 83.3°C/W For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions. b) 47.4°C/W For a device surface mounted on FR4 PCB measured at t ≤ 10 sec.
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSi1Cu0.5
Die attach Method / Material	8200TI EPOXY	**Front metal thickness (Top layer)**	3.0 um
Bond wire material & dia.	Copper wire, 1.7mil	**Back metal type (All layers)**	Ti/Ni/Ag
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	N/A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	None
No. of bonds over active area	5 wires	**Die size (width x length x thickness) in mm**	1.170*1.150*0.229mm
Package material type	EME-G600	**Die passivation thickness range**	N/A
Package material manufacturer	SUMITOMO Bakelite	**No. of mask steps**	7

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Christiana Bob-Manuel	January 10, 2013	Darren Reynolds	January 10, 2013

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary

FACTORY:		PART NUMBER : ZXMN6A11Z SWR1202224 Package Description : SOT89-3L		CUSTOMER: DIODES INC.:		
LABORATORY (If Different):		PART DESCRIPTION : Qualification for Copper Wire Bonding (wafer: 9ZXMN6A11T-CD, 1.7 Cu wire+ EME-G600).				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	385	0/385	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic BVDSS@VGS=0V, ID=250uA Characteristic IDSS@VDS=60V, VGS=0V Characteristic IGSS@VGS=±20V, VDS=0V Characteristic VGS(th)@VDS=VGS, ID=250uA Characteristic RDSON@VGS=4.5V, ID=2.5A Characteristic RDSON@VGS=10V, ID=2.0A Characteristic yFS@VDS=15V,ID=2.5A	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	N/A	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150℃ Vd=60V, PER JESD22 A-108				
	Pretest		1	77	0/77	
	@ 500 Hours	T=150℃ Vd=60V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150℃ Vd=60V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	T=150℃ Vg=20V, PER JESD22 A-108				
	Pretest		1	77	0/77	
	@ 500 Hours	T=150℃ Vg=20V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150℃ Vg=20V, PER JESD22 A-108	1	77	0/77	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55℃-150℃, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55℃-150℃, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55℃-150℃, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121℃ 15PSIG 100%RH				
	Pretest		1	77	0/77	
	Final 96 Hours	T=121℃ 15PSIG 100%RH	1	77	0/77	
7.3.5.7 (9-1)	Highly Accelerated Stress Test(HAST)	T=130℃ RH=85% Vd=42V	1	77		
	Pretest		1	77	0/77	
	Final 96 Hours	T=130℃ RH=85% Vd=42V	1	77	0/77	
7.3.5.7 (9-2)	High Humidity High Temp. Reverse Bias(H^3TRB)	T=85℃ RH=85% Vd=60V	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=85℃ RH=85% Vd=60V	1	77	0/77	
	Final 1000 Hours	T=85℃ RH=85% Vd=60V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vd=5V / Id=250mA; PER MIL-STD-750 METHOD 1037				2mins on/off
	Pretest		1	77	0/77	
	@ 7560 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	Final 15000 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77	N/A	
7.3.5.9 (11)	High Temperature Storage Life (HTSL)	T=150℃, PER JESD22 A-103				
	Pretest		1	45	0/45	
	@ 500 hours	T=150℃, PER JESD22 A-103	1	45	0/45	
	Final 1000 hours	T=150℃, PER JESD22 A-103	1	45	0/45	
7.3.5.9 (12)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	pass	MM=100V HBM=400V
7.3.5.10 (13)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	4	0/4	
7.3.5.11 (14)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (15)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30	N/A	
7.3.5.13 (16)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30	N/A	
(17)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(20)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (21)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260℃@30sec
7.3.5.15 (22)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245℃@5sec
7.3.5.16 (23)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (24)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (25)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (26)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(27)	UNCLAMPED INDUCTIVE SWITCHING (UIS)	N/A, not for Diode	N/A	N/A		
(28)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary: The lot passed the precondition test and 1000hrs hi-rel tests.						
Submitted by: Jianhua Yang 7/26/12		**Approved by: Adam Gu 7/26/12**				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	110C
DIC P/N	ZXMP4A57E6	**Lead material type**	EFTEC-64T
Package Type	SOT-26	**Lead Material manufacturer**	MHT
DIE P/N	ZXMP4A57D	**Lead plating/ coating**	Pb free
Die line or process	MOSFET	**Lead frame material type**	SOT-26C
Wafer Diameter	6 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	OFAB	**Max junction temperature(T_j)**	150C
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	113 °C/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSiCu
Die attach Method / Material	Epoxy/8200TI	**Front metal thickness (Top layer)**	3.0 um
Bond wire material & dia.	Copper wire, 1.7mil	**Back metal type (All layers)**	TiNiAg
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	N/A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	Oxide
No. of bonds over active area	Gate: 1 wire; Source: 3 wires	**Die size (width x length x thickness) in mm**	1.09*1.85*0.229mm
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	Ox/Nitride
Package material manufacturer	HITACHI	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Robert Shen	November 22, 2012	Bill Tian	November 22, 2012
Signature				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Reliability Test Summary

FACTORY:		PART NUMBER : ZXMP4A57E6 SWR1112183 Package Description : SOT-26		CUSTOMER: DIODES INC.:		
LABORATORY (If Different):		PART DESCRIPTION : Qualification for Copper Wire Bonding (wafer: ZXMP4A57D, 1.7 Cu wire+ CEL1702HF9 SK).				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	385	0/385	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=-55*C, Ta2=25*C, Ta3=85*C, Ta4=150*C Characteristic BVDSS@VGS=0V, ID=-250mA Characteristic IDSS@VDS=-40V, VGS=0V Characteristic IGSS@VGS=±20V, VDS=0V Characteristic VGS(th)@VDS=VGS, ID=-250uA Characteristic RDSON@VGS=-4.5V, ID=-10.0A Characteristic RDSON@VGS=-10.0V, ID=-12.0A Characteristic yFS@VDS=-15V,ID=4.0A Characteristic VSD@VDS=VGS,IS=-4A	1 of 3	25	0/25	
	Lot #2		2 of 3	25		
	Lot #3		3 of 3	25		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	1	45	N/A	
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150℃ Vd=40V, PER JESD22 A-108				
	Pretest		1	77	0/77	
	@ 500 Hours	T=150℃ Vd=40V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150℃ Vd=40V, PER JESD22 A-108	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	T=150℃ Vg=20V, PER JESD22 A-108				
	Pretest		1	77	0/77	
	@ 500 Hours	T=150℃ Vg=20V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150℃ Vg=20V, PER JESD22 A-108	1	77	0/77	
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55℃-150℃, PER JESD22 A-104				
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55℃-150℃, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55℃-150℃, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121℃ 15PSIG 100%RH				
	Pretest		1	77	0/77	
	Final 96 Hours	T=121℃ 15PSIG 100%RH	1	77	0/77	
7.3.5.7 (9-1)	Highly Accelerated Stress Test(HAST)	T=130℃ RH=85% Vd=32V	1	77		
	Pretest		1	77	0/77	
	Final 96 Hours	T=130℃ RH=85% Vd=32V	1	77	0/77	
7.3.5.7 (9-2)	High Humidity High Temp. Reverse Bias(H^3TRB)	T=85℃ RH=85% Vd=40V	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=85℃ RH=85% Vd=40V	1	77	0/77	
	Final 1000 Hours	T=85℃ RH=85% Vd=40V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vd=5V / Id=160mA; PER MIL-STD-750 METHOD 1037				2mins on/off
	Pretest		1	77	0/77	
	@ 7560 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	Final 15000 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	1	77	N/A	
7.3.5.9 (11)	High Temperature Storage Life (HTSL)	T=150℃, PER JESD22 A-103				
	Pretest		1	45	0/45	
	@ 500 hours	T=150℃, PER JESD22 A-103	1	45	0/45	
	Final 1000 hours	T=150℃, PER JESD22 A-103	1	45	0/45	
7.3.5.9 (12)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	pass	MM=150V HBM=500V
7.3.5.10 (13)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	6	0/6	
7.3.5.11 (14)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (15)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	1	30	N/A	
7.3.5.13 (16)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	1	30	N/A	
(17)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(20)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (21)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260℃@30sec
7.3.5.15 (22)	SOLDERABILITY (SD)	J-STD-002	1	10	0/10	245℃@5sec
7.3.5.16 (23)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (24)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (25)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (26)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(27)	UNCLAMPED INDUCTIVE SWITCHING (UIS)	N/A, not for Diode	N/A	N/A		
(28)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary: The lot passed the precondition test and 1000hrs hi-rel tests.						
Submitted by: Jianhua Yang 4/16/12		**Approved by: Adam Gu 4/16/12**				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	ZXT13P20DE6TA	**Lead material type**	EFTEC-64T
Package Type	SOT-26	**Lead Material manufacturer**	MHT
DIE P/N	CY5T2D	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-26C
Wafer Diameter	6 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Kfab	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	113℃
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSiCu
Die attach Method / Material	EPOXY/8200TI	**Front metal thickness (Top layer)**	6.0um
Bond wire material & dia.	Copper Wire,1.7 mil	**Back metal type (All layers)**	Ti/Ni/Ag
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	4	**Die size (width x length x thickness) in mm**	1.727*0.838*0.178mm
Package material type	CEL-1702HF9SK	**Die passivation thickness range**	N/A
Package material manufacturer	HITACHI	**No. of mask steps**	6

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

	Completed by	Date	Certified by	Date
Typed/Printed	Yoyo Tan	April 22, 2013	Bill Tian	April 22, 2013
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: ZXT13P20DE6TA SWR1302131 CUSTOMER: Package: SOT26 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION: KFAB Wafer:CY2D 50128403,1.7mil Cu wire + CEL-1702HF9 SKF				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125, Ta4=150 BVCEO@IC= 10.0mA ICBO @VCB= -20V HFE@VCE= -2V,IC= -1A VCESAT@IC= -1A,IB= -100mA	1	25	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150°C Vc=40V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150°C Vc=40V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150°C Vc=40V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150°C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150°C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150°C , PER JESD22A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55°C-150°C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121°C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85°C RH=85% Vc=64V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85°C RH=85% Vc=64V	N/A	N/A		
	Final 1000 Hours	T=85°C RH=85% Vc=64V	N/A	N/A		Remark1
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130°C RH=85% Vc=40V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130°C RH=85% Vc=40V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=15V Ic=60mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260°C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 05/30/13	Approved by: Adam Gu 05/30/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	ZXTN2005GTA	**Lead material type**	CDA 194
Package Type	SOT-223	**Lead Material manufacturer**	VAST/XMYH
DIE P/N	CY869D	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-223A
Wafer Diameter	6 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Kfab	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	78℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSCui
Die attach Method / Material	SOFT-SOLDER/Pb92.5Sn5Ag2.5	**Front metal thickness (Top layer)**	6um
Bond wire material & dia.	Copper Wire,1.7 mil	**Back metal type (All layers)**	Ti/Ni/Ag
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	3	**Die size (width x length x thickness) in mm**	1.295*1.295*0.229mm
Package material type	EME-G600	**Die passivation thickness range**	N/A
Package material manufacturer	SUMITOMO	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

	Completed by	Date	Certified by	Date
Typed/Printed	Yoyo Tan	April 22, 2013	Bill Tian	April 22, 2013
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: ZXTN2005GTA SWR1302140 CUSTOMER: Package: SOT223 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION: KFAB Wafer:CY869D 50128120,1.7mil Cu wire + EME-G600				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125, Ta4=150 BVCBO@IC= 100uA ICBO @VCB=50V HFE@VCE= 1V,IC= 1A	1	25	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vc=48V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vc=48V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vc=48V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150*C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150*C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150*C , PER JESD22A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=64V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85*C RH=85% Vc=64V	N/A	N/A		
	Final 1000 Hours	T=85*C RH=85% Vc=64V	N/A	N/A		Remark1
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130*C RH=85% Vc=40V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130*C RH=85% Vc=40V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=30V Ic=30mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	4	0/4	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260*C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot has passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 05/30/13	Approved by: Adam Gu 05/30/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	ZXTN25012EFH	**Lead material type**	CDA194
Package Type	SSOT-23	**Lead Material manufacturer**	PBE / Hitachi
DIE P/N	CZ25N12ED	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-23R
Wafer Diameter	6 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	KFAB	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	171℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	AlSiCu
Die attach Method / Material	EPOXY	**Front metal thickness (Top layer)**	6um
Bond wire material & dia.	Copper Wire, 1.7mil	**Back metal type (All layers)**	TiNiAg
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	4	**Die size (width x length x thickness) in mm**	0.81*0.81*0.178
Package material type	KTMC1050G	**Die passivation thickness range**	No
Package material manufacturer	KCC	**No. of mask steps**	5

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	February 22, 2013	Bill Tian	February 22, 2013

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: ZXTN25012EFHTA SWR1111106 CUSTOMER: Package: SOT23 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION: KFAB wafer:CZ25N12ED 50089366,1.7mil Copper wire+KTMC1050G+8200TI				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	600	0/600	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125, Ta4=150 BVCEO@IC= 10.0mA ICBO @VCB= 64V HFE@VCE= 5V,IC= 1A VCESAT@IC= 1A,IB= 100mA	N/A	N/A		
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150°C Vc=16V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150°C Vc=16V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150°C Vc=16V, PER JESD22 A-108	1	77	0/77	
7.3.5.4(6)	HIGH TEMP. Storage Life (HTS)	T=150°C , PER JESD22 A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150°C , PER JESD22 A-103	1	45	0/45	
	Final 1000 Hours	T=150°C , PER JESD22 A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55°C-150°C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55°C-150°C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121°C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85°C RH=85% Vc=48V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85°C RH=85% Vc=48V	N/A	N/A		
	Final 1000 Hours	T=85°C RH=85% Vc=48V	N/A	N/A		
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130°C RH=85% Vc=16V,PER JESD22 A-110	1	77	0/77	
	Pretest		1	77	0/77	
	After 96hrs	T=130°C RH=85% Vc=16V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=10V Ic=60mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	4	0/4	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260°C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245°C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A		
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 03/12/12	Approved by: Adam Gu 03/12/12				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Printed specifications are not controlled documents. Verify revision before using.

Assembly and Test Site	DIODES INC	**Glass Transition Temperature (T_G)**	130℃
DIC P/N	ZXTP23140BFH	**Lead Frame Type**	SOT-23R
Package Type	SSOT-23	**Lead Frame Manufacturer**	PBE / Hitachi
DIE P/N	CZ23P60BD	**Lead Frame Material**	CDA194FH
Die Line or Process	Transistor	**Terminal Finish (Plating) Material**	Pb free
Wafer Diameter	6 inch	**Header Plating (Die Land Area)**	Silver Spot Plate
Wafer Fab Site(s)	KFAB	**Max Junction Temperature (T_j)**	150℃
ID Method (multiple sites)	N/A	**Max Thermal Resistance Junction to Case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max Thermal Resistance Junction to Ambient (θ_{JA})***	171℃
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front Metal Type (Top Layer)**	AlSiCu
Die attach Method / Material	EPOXY/8200TI	**Front Metal Thickness (Top Layer)**	6.0 um
Bond Wire/Clip Material & Wire Diameter	Copper Wire,1.7 mil	**Back Metal Type (All Layers)**	Ti/Ni/Ag
Bond Type (at top side of the die)	Thermo sonic	**Back Metal Thickness (all Layers)**	N/A
Bond Type (at leadframe)	Thermo sonic	**Die Conformal Coating (Passivation)**	N/A
No. of Bonds over Active Area	4	**Die Passivation Thickness Range**	N/A
Mold Compound Material Type	CEL-1702HF9 SK	**Die Size (Width x Length x Thickness) in mm**	1.83*0.82*0.178mm
Mold Compound Material Manufacturer	HITACHI	**No. of Mask Steps**	6

Completed by		**Date**	**Certified by**	**Date**
Typed/Printed	Yoyo Tan	July 25, 2013	Bill Tian	July 25, 2013
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: ZXTP23140BFH SWR1305233 CUSTOMER: Package: SOT23 DIODES INC.:				
LABORATORY (If Different):		PART DESCRIPTION: KFAB wafer:CZ23P60BD 50128127,1.7mil Cu wire+CEL-1702HF9 SKF				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	500	0/500	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125C, Ta4=150C BVCBO @IC=-100uA ICBO @VCB=-130V HFE @Vce=-5V,Ic=-10mA Vcesat @Ic=-100mA,Ib=-5mA	1	25	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=80*C Vc=128V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=80*C Vc=128V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=80*C Vc=128V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150*C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150*C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150*C , PER JESD22A-103	1	45	0/45	
7.3.6.5(6)	HAST	T=130*C RH=85% Vc=42V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	@ 96 Hours	T=130*C RH=85% Vc=42V	1	77	0/77	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=40V,PER JESD22 A-101	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85*C RH=85% Vc=40V	N/A	N/A		
	Final 1000 Hours	T=85*C RH=85% Vc=40V	N/A	N/A		
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=60V Ic=10mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000 Cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	4	0/4	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260*C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot has passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 09/03/13	Approved by: Susan Ding 09/03/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	ZXTP25020DZTA	**Lead material type**	CDA194FH
Package Type	SOT-89	**Lead Material manufacturer**	VAST/XMYH
DIE P/N	X25P20DXD	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT89-3L
Wafer Diameter	6 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Ofab	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	N/A
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-Si,
Die attach Method / Material	EPOXY/8200TI	**Front metal thickness (Top layer)**	6.0um
Bond wire material & dia.	Copper Wire,1.5 mil	**Back metal type (All layers)**	Ti/Ni/Ag
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	NA
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	4	**Die size (width x length x thickness) in mm**	0.81*0.81*0.229mm
Package material type	EME-G600	**Die passivation thickness range**	N/A
Package material manufacturer	SUMITOMO	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

	Completed by	Date	Certified by	Date
Typed/Printed	Yoyo Tan	August 30, 2012	Bill Tian	August 30, 2012
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: ZXTP25020DZTA SWR1108190 Package: SOT89-3L			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: Zetex wafer:X25P20DXD 9N37SARAN.4,1.5mil Copper wire+EME-G600				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	600	0/600	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125, Ta4=150 BVCEO@IC= 10.0mA ICBO @VCB= 64V HFE@VCE= 5V,IC= 1A VCESAT@IC= 1A,IB= 100mA	N/A	N/A		
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vc=20V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vc=20V, PER JESD22 A-108	1	77	0/77	
	Final 1000 Hours	T=150*C Vc=20V, PER JESD22 A-108	1	77	0/77	
7.3.5.4(6)	HIGH TEMP. Storage Life (HTS)	T=150*C , PER JESD22 A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150*C , PER JESD22 A-103	1	45	0/45	
	Final 1000 Hours	T=150*C , PER JESD22 A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=64V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85*C RH=85% Vc=64V	N/A	N/A		
	Final 1000 Hours	T=85*C RH=85% Vc=64V	N/A	N/A		
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130*C RH=85% Vc=20V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130*C RH=85% Vc=20V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=15V Ic=40mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint 7560cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
	After 15000cycles	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	N/A	N/A		MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	N/A	N/A		
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	1	30	0/30	
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF)	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260*C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245*C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	N/A	N/A		
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	1	25	0/25	
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	1	25	0/25	
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 12/12/11	Approved by: Adam Gu 12/12/11				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Printed specifications are not controlled documents. Verify revision before using.

Assembly and Test Site	DIODES INC	**Glass Transition Temperature (T_G)**	130℃
DIC P/N	ZXTP25020DZTA	**Lead Frame Type**	SOT89-3L
Package Type	SOT-89	**Lead Frame Manufacturer**	VAST/XMYH
DIE P/N	CZ25P20DXD	**Lead Frame Material**	CDA194FH
Die Line or Process	Transistor	**Terminal Finish (Plating) Material**	Pb free
Wafer Diameter	6 inch	**Header Plating (Die Land Area)**	Silver Spot Plate
Wafer Fab Site(s)	KFAB	**Max Junction Temperature (T_j)**	150℃
ID Method (multiple sites)	N/A	**Max Thermal Resistance Junction to Case (θ_{JC})**	N/A
Assembly Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max Thermal Resistance Junction to Ambient (θ_{JA})***	150℃/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front Metal Type (Top Layer)**	AlSiCu
Die attach Method / Material	EPOXY/8200TI	**Front Metal Thickness (Top Layer)**	6 um
Bond Wire/Clip Material & Wire Diameter	Copper Wire,1.7 mil	**Back Metal Type (All Layers)**	Ti/Ni/Ag
Bond Type (at top side of the die)	Thermo sonic	**Back Metal Thickness (all Layers)**	N/A
Bond Type (at leadframe)	Thermo sonic	**Die Conformal Coating (Passivation)**	N/A
No. of Bonds over Active Area	4	**Die Passivation Thickness Range**	N/A
Mold Compound Material Type	EME-G600	**Die Size (Width x Length x Thickness) in mm**	0.81*0.81*0.229mm
Mold Compound Material Manufacturer	SUMITOMO	**No. of Mask Steps**	6

Completed by		**Date**	**Certified by**	**Date**
Typed/Printed	Yoyo Tan	July 24, 2013	Bill Tian	July 24, 2013
Signature				
Title				

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: ZXTP25020DZTA SWR1305068 Package: SOT89-3L			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: KFAB wafer:CZ25P20DXD 50134644,Cu 1.5mil + EME-G600				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	385	0/385	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	600	0/600	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125c, Ta4=150c BVCBO@IC=-100uA ICBO @VCB=-25V HFE@VCE= -2V,IC= -1A	1	25	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vc=20V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vc=20V, PER JESD22 A-108	1	77	0/77	
	Final 1000Hours	T=150*C Vc=20V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150*C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150*C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150*C , PER JESD22A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=48V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85*C RH=85% Vc=48V	N/A	N/A		
	Final 1000 Hours	T=85*C RH=85% Vc=48V	N/A	N/A		
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130*C RH=85% Vc=20V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130*C RH=85% Vc=20V,PER JESD22 A-110	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=15V Ic=60mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2mins on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/60	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	4	0/4	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260*C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245*C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	N/A	N/A		
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UI	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 08/14/13	Approved by: Adam Gu 08/14/13				

CERTIFICATE OF DESIGN AND CONSTRUCTION

Assembly and Test Site	DIODES INC	**Glass transition temperature (T_G)**	130℃
DIC P/N	ZXTP749FTA	**Lead material type**	CDA194
Package Type	SSOT-23	**Lead Material manufacturer**	PBE / Hitachi
DIE P/N	X26P25CYD	**Lead plating/ coating**	Pb free
Die line or process	Transistor	**Lead frame material type**	SOT-23R(SSOT-23)
Wafer Diameter	6 inch	**Header plating (Die land area)**	Silver Spot Plate
Wafer Fab Site(s)	Ofab	**Max junction temperature(T_j)**	150℃
ID method (multiple sites)	N/A	**Max thermal resistance junction to case (θ_{JC})**	N/A
Assembly Locations(s)	Shanghai Kaihong Electronic Co., Ltd. No.999 Chenchun Road, Xinqiao Town, Songjiang,Shanghai,P.R. China 201612 DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Max thermal resistance junction to ambient (θ_{JA})***	172°C/W
Test Locations(s)	DIODES INC. IN SHANGHAI, Plant1,NO.111-10 Songjiang Export Processing Zone, Shanghai,P.R.China 201600	**Front metal type (Top layer)**	Al-Si
Die attach Method / Material	EPOXY/8200TI	**Front metal thickness (Top layer)**	6um
Bond wire material & dia.	Copper Wire, 1.3mil	**Back metal type (All layers)**	Ti/Ni/Ag
Bond type (at top side of the die)	Thermo sonic	**Back metal thickness (all Layers)**	300-2600-5500 A
Bond type (at leadframe)	Thermo sonic	**Die conforming coating**	NA
No. of bonds over active area	2	**Die size (width x length x thickness) in mm**	0.74*0.77*0.203
Package material type	GR640HV-L1	**Die passivation thickness range**	No
Package material manufacturer	Henkel	**No. of mask steps**	N/A

*Show conditions (i.e. pad size, board material, copper thickness, etc.

Attachments:

1) Die Photo

2) Package outline drawing

3) Die cross-section drawing
4) Wire bond & die placement diagram
5) Test circuits, bias levels and conditions

Requirements:

A separate Certificate of Design, Construction and Qualification shall be submitted for each P/N and assembly location.
Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct. Type name and sign.

Completed by		Date	Certified by	Date
Typed/Printed	Yoyo Tan	November 16, 2012	Bill Tian	November 16, 2012

SHANGHAI KAIHONG ELECTRONIC CO.,LTD

Hi-Reliability Test Summary Report

FACTORY:		PART NUMBER: ZXTP749FTA SWR1205118 Package: SOT23			CUSTOMER: DIODES INC.:	
LABORATORY (If Different):		PART DESCRIPTION: OFAB Wafer:X26P25CYD 9P39DORTY.8, Cu 1.0mil + GR640HV-L1				
DW-008 (AEC Q101) Test#	Test Description	Test Conditions	#Lots	#To Test	**Results**	REMARKS
7.3.2 (1)	PRE- AND POST- STRESS ELECTRICAL TEST (TEST)	Per Spec				
7.3.3 (2)	PRECONDITIONING (PC)	JSED22 A-113 N/A for Axial	1	308	0/308	
7.3.5.1 (3)	EXTERNAL VISUAL (EV)	MIL-STD-750 METHOD 2071	1	600	0/600	
7.3.5.2 (4)	PARAMETRIC VERIFICATION (PV)	Per Data Sheet Ta1=25C, Ta2=85C, Ta3=125C, Ta4=150C BVCBO @IC=-100uA ICBO @VCB=-28V HFE @Vce=-2V,Ic=-100mA Vcesat @Ic=-1A,Ib=-100mA	1	25	0/25	
	Lot #2		N/A	N/A		
	Lot #3		N/A	N/A		
7.3.5.3	FORWARD SURGE	MIL-750D, Method 4066	N/A	N/A		
7.3.5.4 (5)	HIGH TEMP. REVERSE BIAS (HTRB)	T=150*C Vc=28V, PER JESD22 A-108	1	77		
	Pretest		1	77	0/77	
	@ 500 Hours	T=150*C Vc=28V, PER JESD22 A-108	1	77	0/77	
	Final	T=150*C Vc=28V, PER JESD22 A-108	1	77	0/77	
7.3.5.4 (6)	HIGH TEMP. STORAGE LIFE (HTS)	T=150*C , PER JESD22A-103	1	45		
	Pretest		1	45	0/45	
	@ 500 Hours	T=150*C , PER JESD22A-103	1	45	0/45	
	Final 1000Hours	T=150*C , PER JESD22A-103	1	45	0/45	
(6)	HIGH TEMP GATE BIAS (HTGB)	N/A for Diode	N/A	N/A		
7.3.5.5 (7)	TEMPERATURE CYCLING (TC)	T=-55*C-150*C, PER JESD22 A-104	1	77		
	Pretest		1	77	0/77	
	@ 500 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
	Final 1000 Cycles	T=-55*C-150*C, PER JESD22 A-104	1	77	0/77	
7.3.5.6 (8)	AUTOCLAVE (AC)	T=121*C 15PSIG 100%RH	1	77	0/77	96hrs
7.3.5.7 (9)	H^3TRB	T=85*C RH=85% Vc=60V	N/A	N/A		
	Pretest		N/A	N/A		
	@ 500 Hours	T=85*C RH=85% Vc=60V	N/A	N/A		
	Final 1000 Hours	T=85*C RH=85% Vc=60V	N/A	N/A		
7.3.5.7 (9a)	Highly Accelerated Stress Test(HAST)	T=130*C RH=85% Vc=28V,PER JESD22 A-110	1	77		
	Pretest		1	77	0/77	
	After 96hrs	T=130*C RH=85% Vc=28V	1	77	0/77	
7.3.5.8 (10)	INTERMITTENTOPERATING LIFE (IOL)	Vc=20V Ic=30mA, PER MIL-STD-750 METHOD 1037	1	77		15000cycles@2min s on/off
	Pretest	MIL-STD-750 METHOD 1037	1	77	0/77	
	Midpoint	MIL-STD-750 METHOD 1037	1	77	0/77	
	After	MIL-STD-750 METHOD 1037	1	77	0/77	
(10a)	POWER AND TEMP. CYCLE (PTC)	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
(Optional)	Pretest	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	Midpoint	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
	After	JESD22 A-105, Per Table AEC-Q101, p11	N/A	N/A		
7.3.5.9 (11)	ESD CHARACTERIZATION (ESD)	PER AEC-Q101-001 & -002	1	60	0/10 0/10	MM 400V HBM 8KV
7.3.5.10 (12)	D.P.A. (DPA)	AEC Q101-004 SEC. 4	1	4	0/4	
7.3.5.11 (13)	PHYSICAL DIMENSION (PD)	PER JESD22 B-100	N/A	N/A		
7.3.5.12 (14)	TERMINAL STRENGTH (TS)	MIL-STD-750, Method 2036	N/A	N/A		
7.3.5.13 (15)	RESISTANCE TO SOLVENTS (RTS)	JESD22 B-107	N/A	N/A		
(16)	CONSTANT ACCELERATION (CA)	N/A, not hermetically sealed device.	N/A	N/A		
(17)	VIBRATION VARIABLE FREQUENCY (VVF	N/A, not hermetically sealed device.	N/A	N/A		
(18)	MECHANICAL SHOCK (MS)	N/A, not hermetically sealed device.	N/A	N/A		
(19)	HERMETICITY (HER)	N/A, not hermetically sealed device.	N/A	N/A		
7.3.5.14 (20)	RESISTANCE TO SOLDER HEAT (RSH)	JESD22 B-106	1	45	0/45	260*C@10sec
7.3.5.15 (21)	SOLDERABILITY (SD)	J-STD-002	N/A	N/A		245*C@5sec
7.3.5.16 (22)	THERMAL RESISTANCE (TR)	JESD 24-3, 24-4, 24-6 as appropriate	1	10	0/10	
7.3.5.17 (23)	WIRE BOND STRENGTH (WBS)	MIL-STD-750 METHOD 2037	1	25	0/25	
7.3.5.18 (24)	BOND SHEAR (BS)	AEC-Q101-003	N/A	N/A		
7.3.5.19 (25)	DIE SHEAR (DS)	MIL-STD-750 METHOD 2017	N/A	N/A		
(26)	UNCLAMPED INDUCTIVE SWITCHING (UIS	N/A, not for Diode	N/A	N/A		
(27)	DIELECTRIC INTEGRITY (DI)	N/A, not for Diode	N/A	N/A		
Summary:	This lot passed 1000hrs hi-rel test.					
Submitted by:	Sean Huang 09/29/12	Approved by: Adam Gu 09/29/12				